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A

HSF Property : Comply iSupplier SYSTEM HSF PROPERTY ATTRIBUTE UP-TO DATE VALUE

B

C

HELLO

AMD-Sabine 14"

MV (DISCRETE)

2011/4/28

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DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER	David Cheng		Su Albert	
DESIGN	Ben Wang			
CHECK				
RESPONSIBLE				
SIZE = 3 VER : A02				
FILE NAME : HELLO-6050A2424901-DIS-A01-6L-EE				
P/N	6050A2424901			

INVENTEC			
TITLE Hello AMD discrete Project Name			
SIZE A3	CODE CS	DOC NUMBER I310A24249-0-MTR	REV A02
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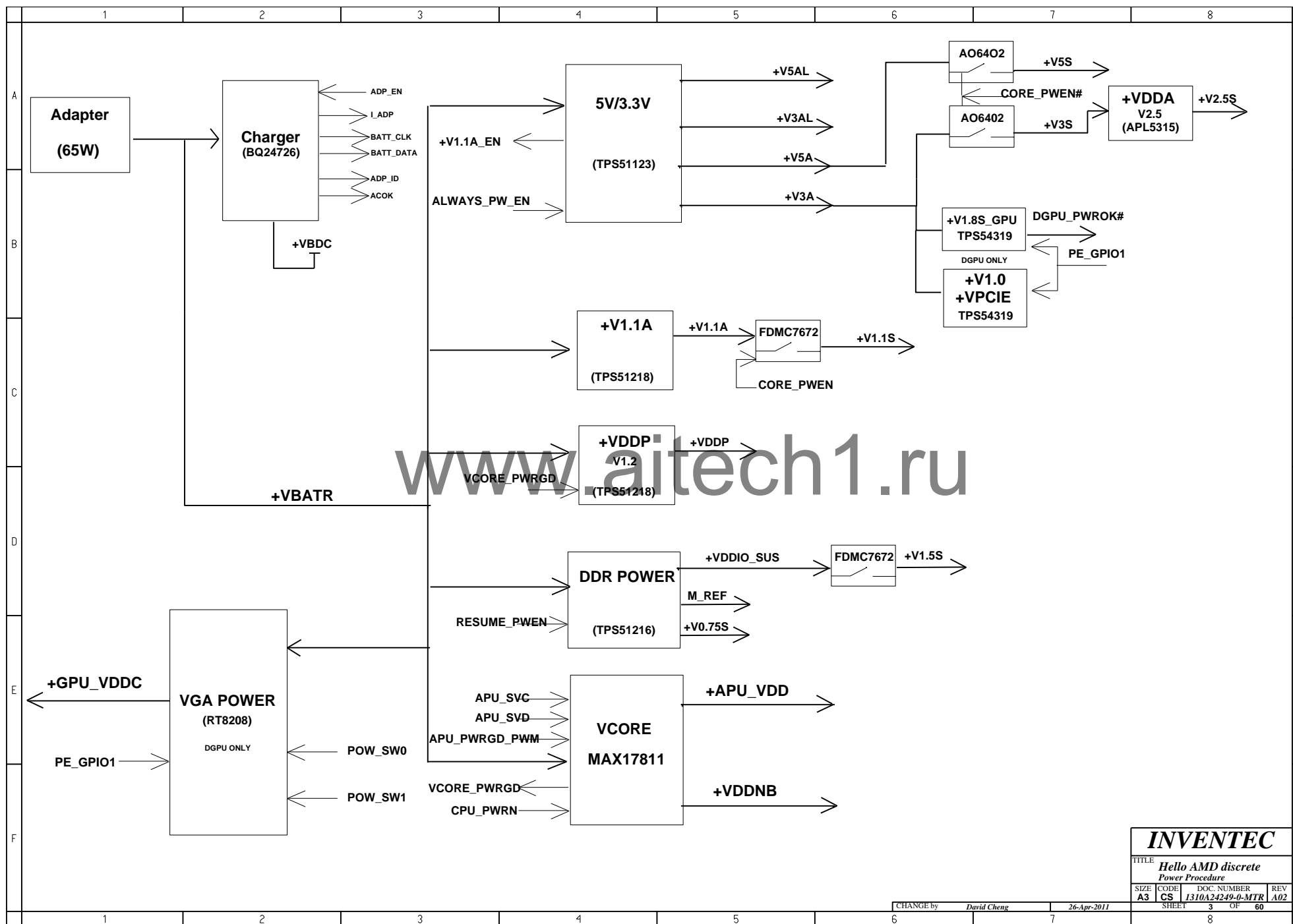
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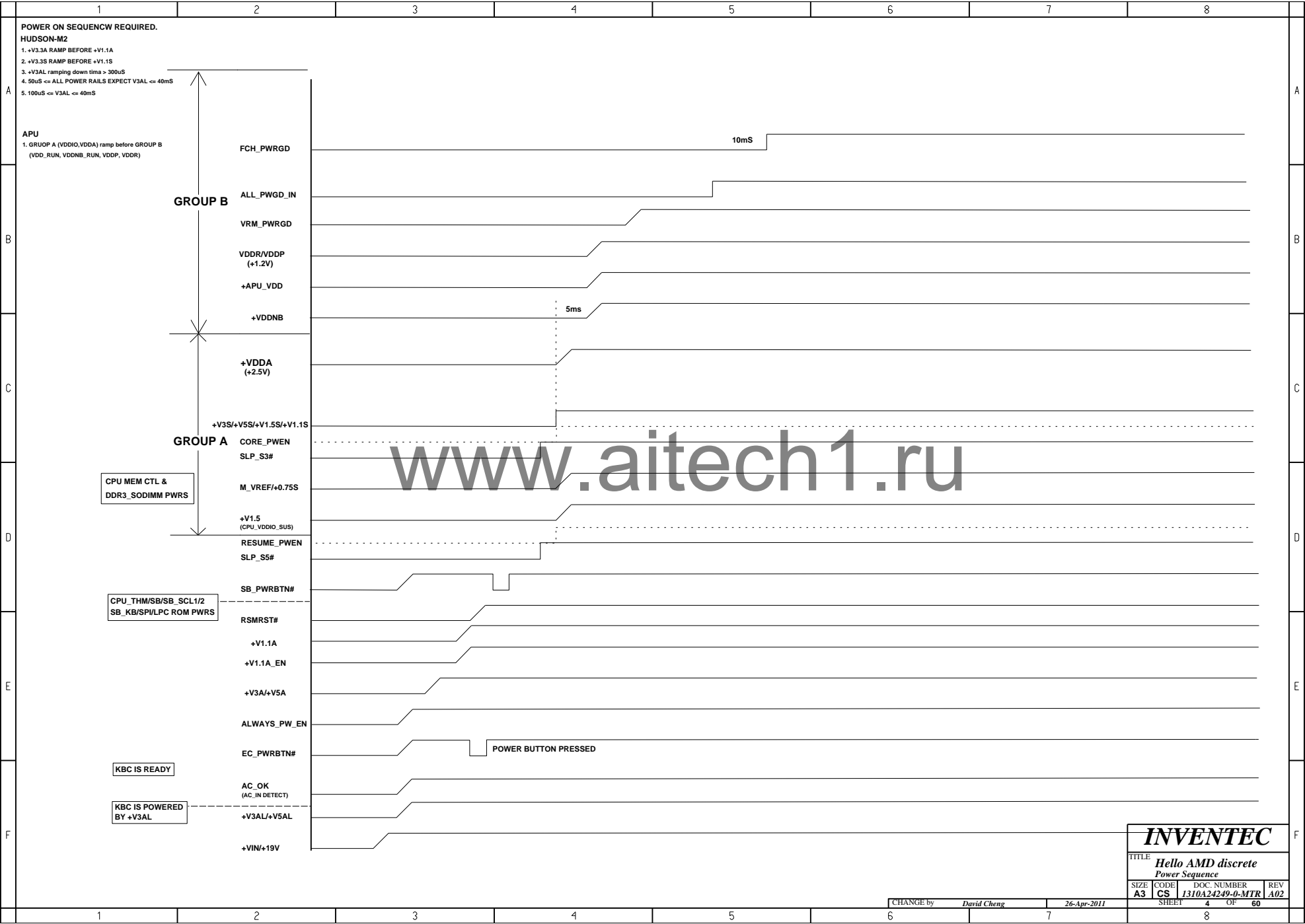
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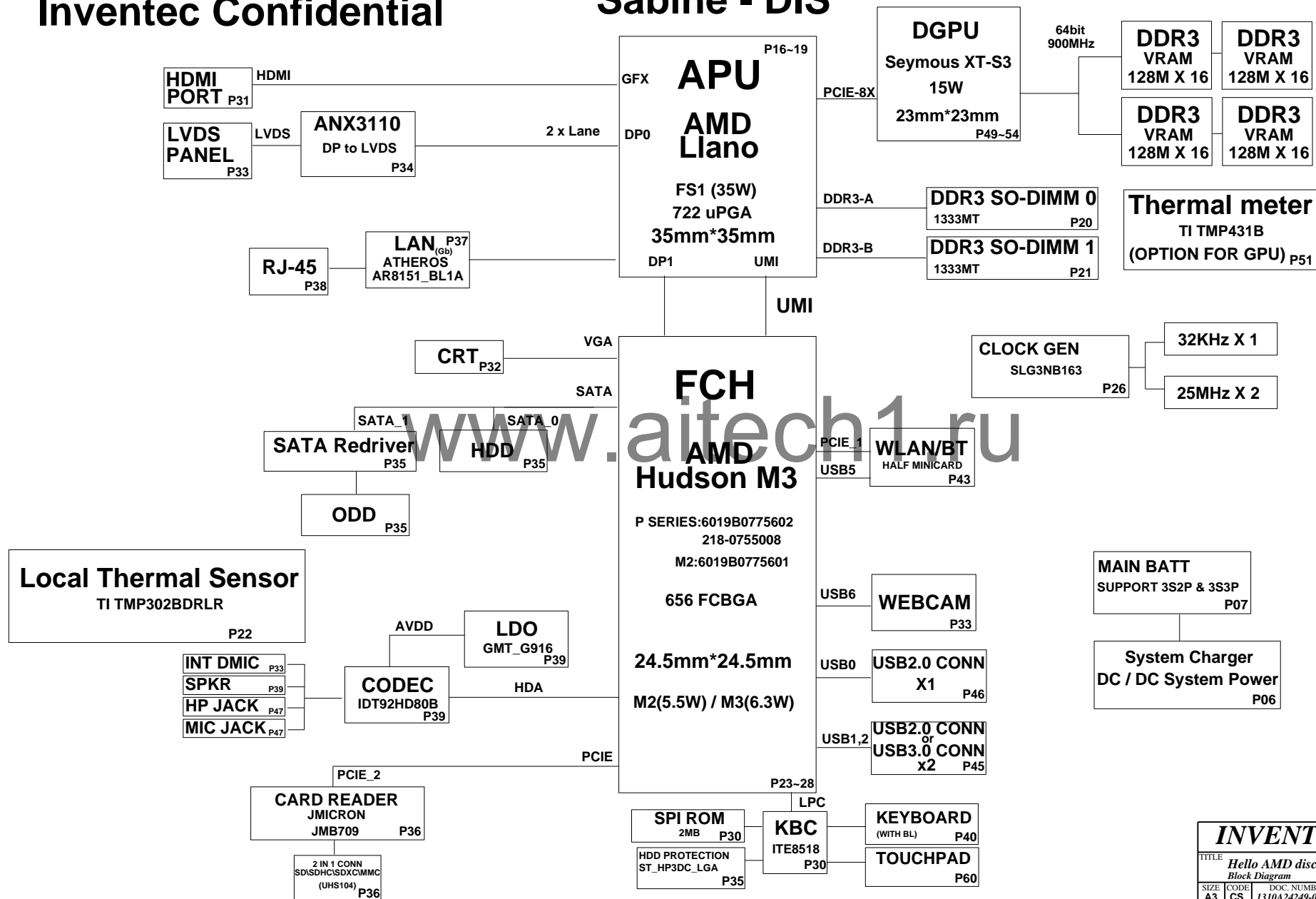
CHANGE by David Cheng 26-Apr-2011





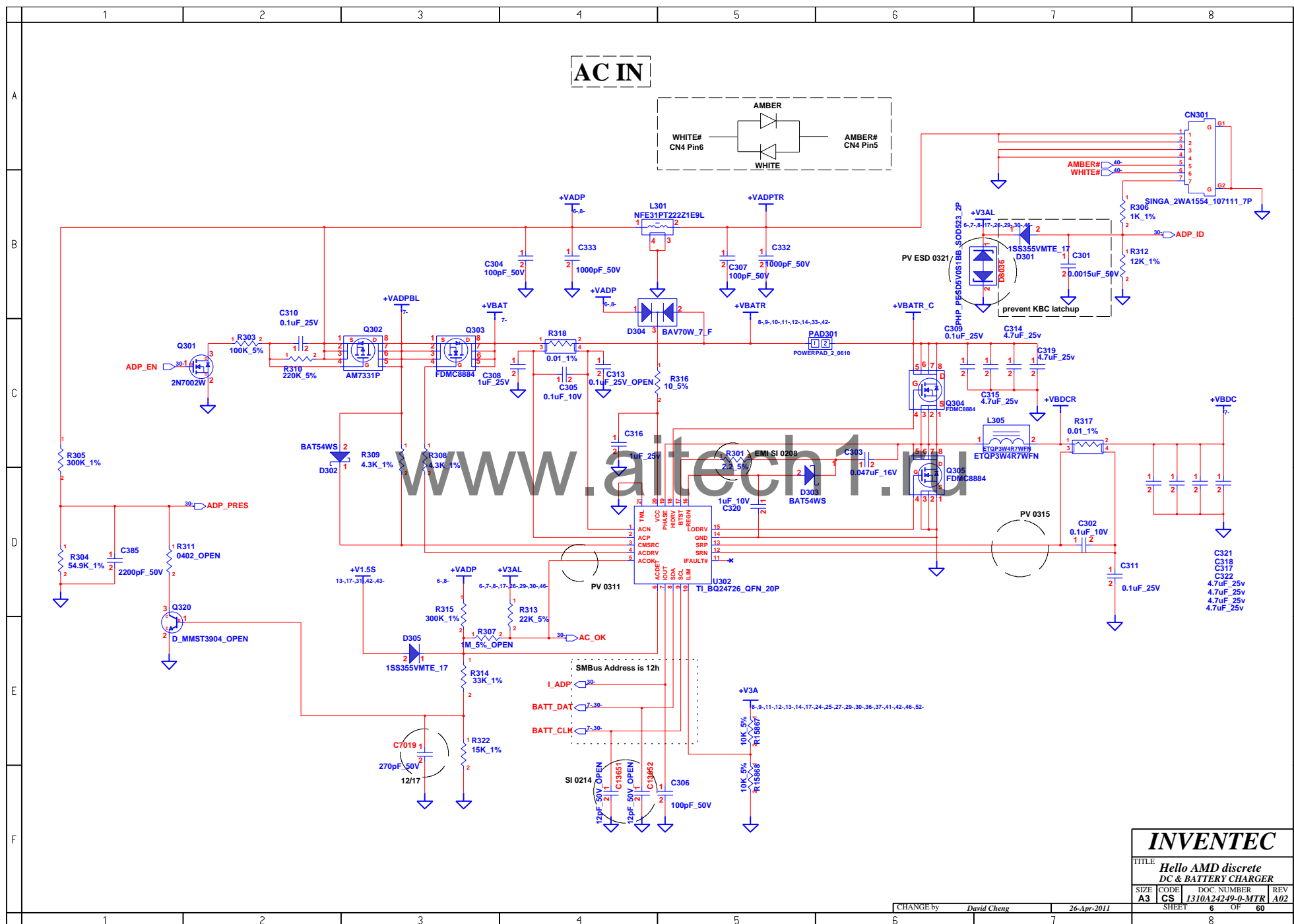
Inventec Confidential

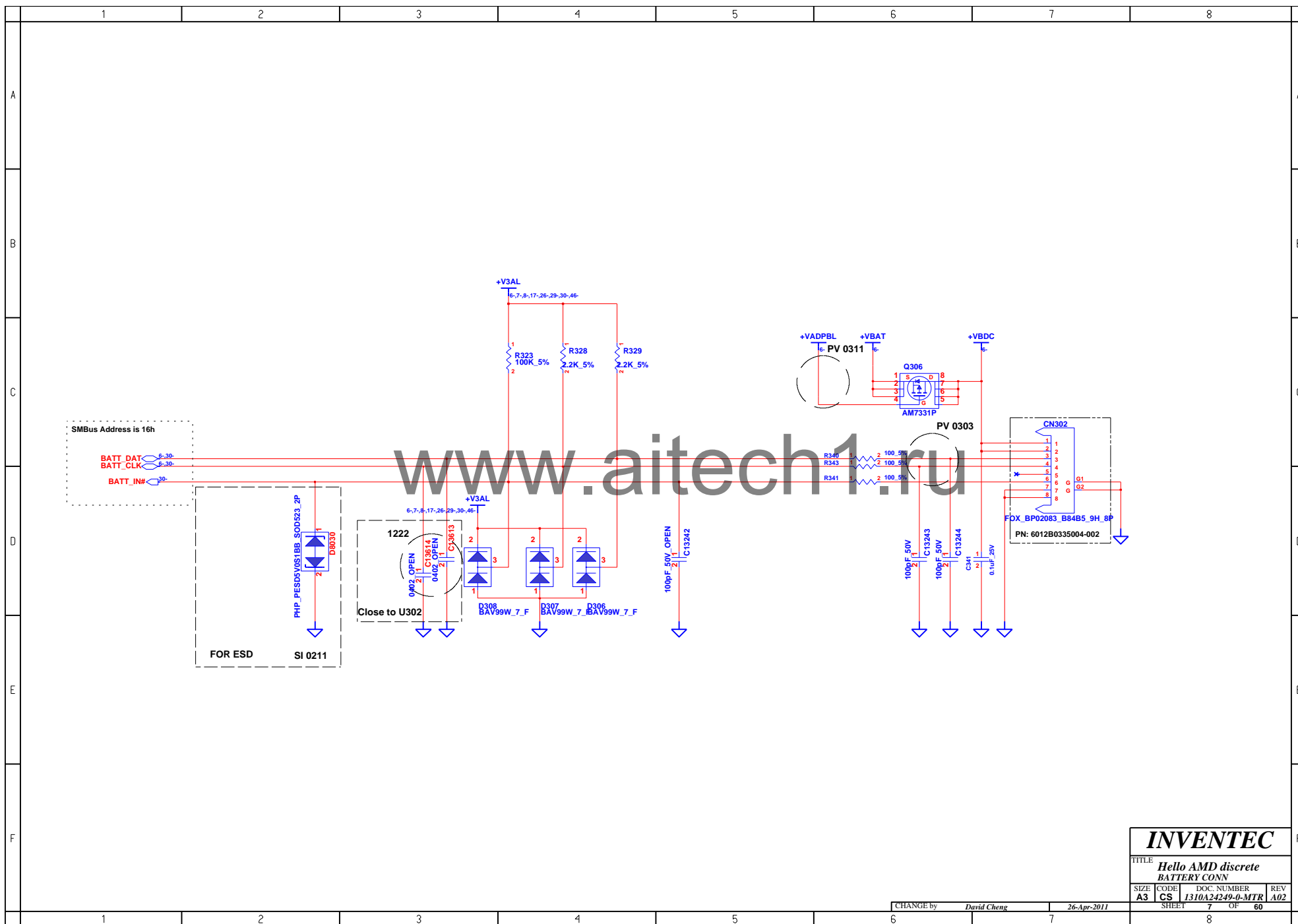
Sabine - DIS



CHANGE by David Cheng 26-Apr-2011

INVENTEC			
TITLE Hello AMD discrete Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310A24249-0-MTR	REV A02
SHEET 5		OF 60	





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TITLE			
<i>Hello AMD discrete</i> +V3A & +V5A			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24249-0-MTR	A02
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CS	1310A24249-0-MTR		
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AC-0.34A
DC-0.598A



TITLE			
<i>Hello AMD discrete</i> <i>+VI.1A & +VDDA</i>			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24249-0-MTR	A02
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CS	1310A24249-0-M1R		
SHEET	9	OF	60

VDDIO_SUS & +V0.75S

AC-1.044A
DC-1.837A

NOTE: DDR3 REGULATOR

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TITLE			
Hello AMD discrete			
+VDDIO_SUS & +V0.75S			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24249-0-MTR	A02
SHEET		10	OF 60

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VDDIO_SUS & +V0.75S

AC-1.044A
DC-1.837A

NOTE: DDR3 REGULATOR

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TITLE			
Hello AMD discrete			
+VDDIO_SUS & +V0.75S			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24249-0-MTR	A02
SHEET		10	OF 60

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VDDIO_SUS & +V0.75S

AC-1.044A
DC-1.837A

VDDIO_SUS & +V0.75S

AC-1.044A
DC-1.837A

VDDIO_SUS & +V0.75S

AC-1.044A
DC-1.837A

I MAX = 14A

NOTE: DDR3 REGULATOR

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TITLE Hello AMD discrete
+VDDIO_SUS & +V0.75S

SIZE A3 CODE CS DOC NUMBER 1310A24249-0-MTR REV A02

SHEET 10 OF 60

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VDDIO_SUS & +V0.75S

AC-1.044A
DC-1.837A

VDDIO_SUS & +V0.75S

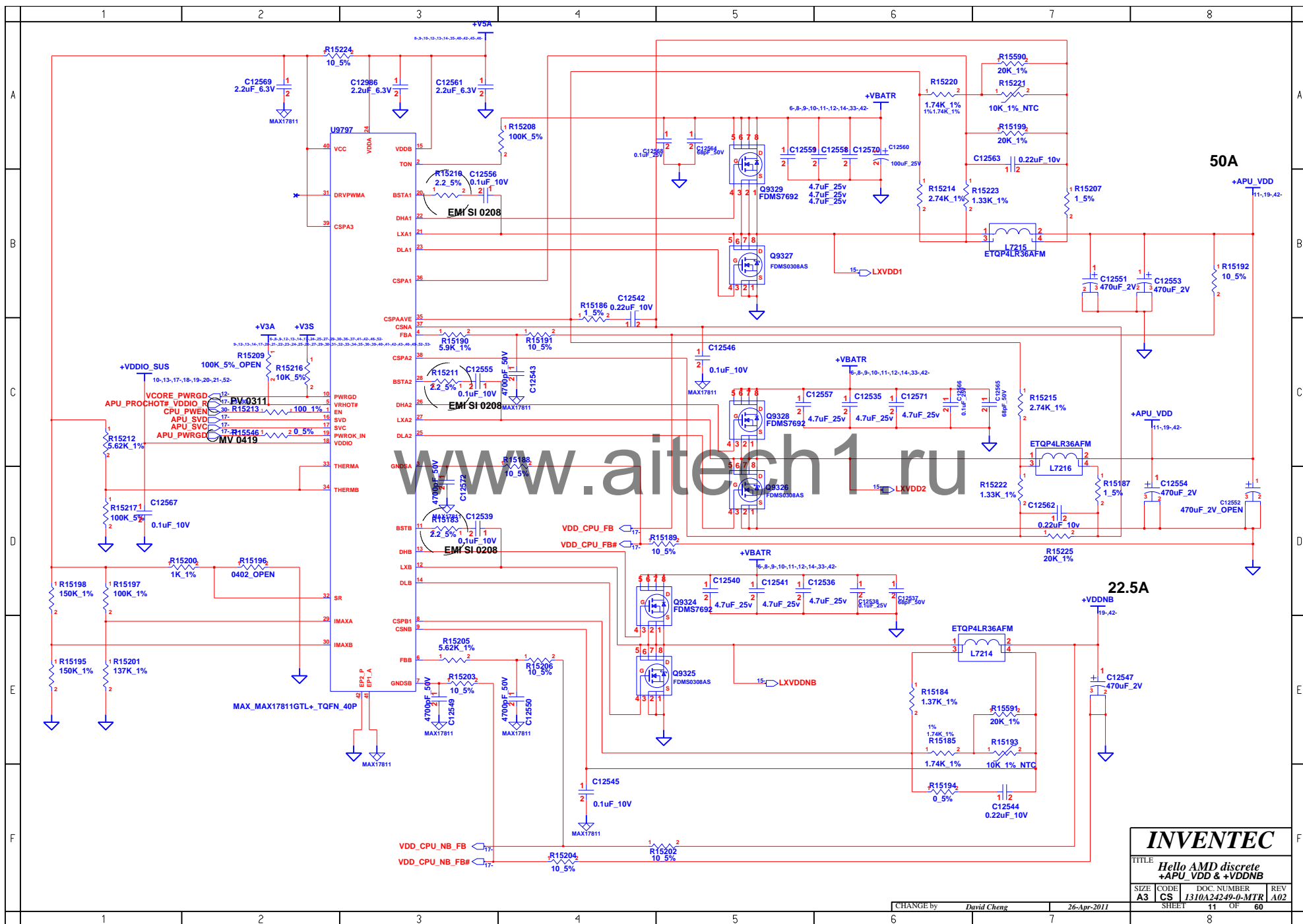
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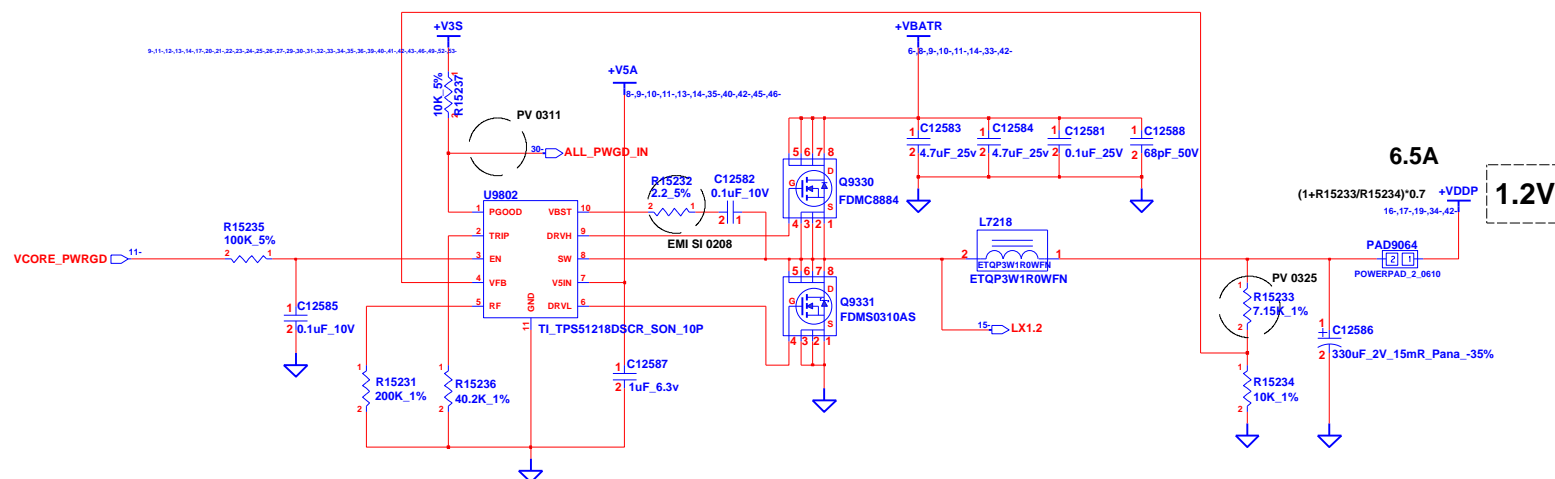
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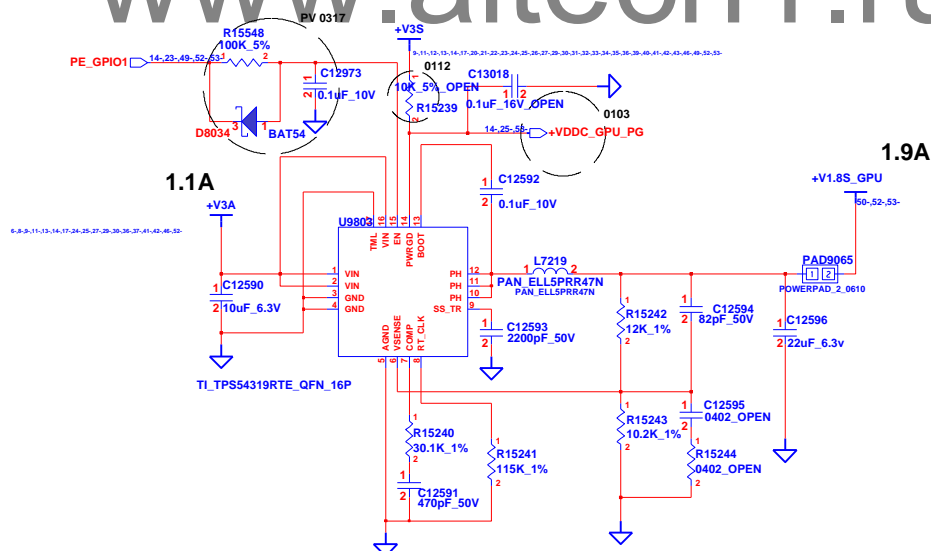
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DC-1.837A



AC-0.357A
DC-0.83A



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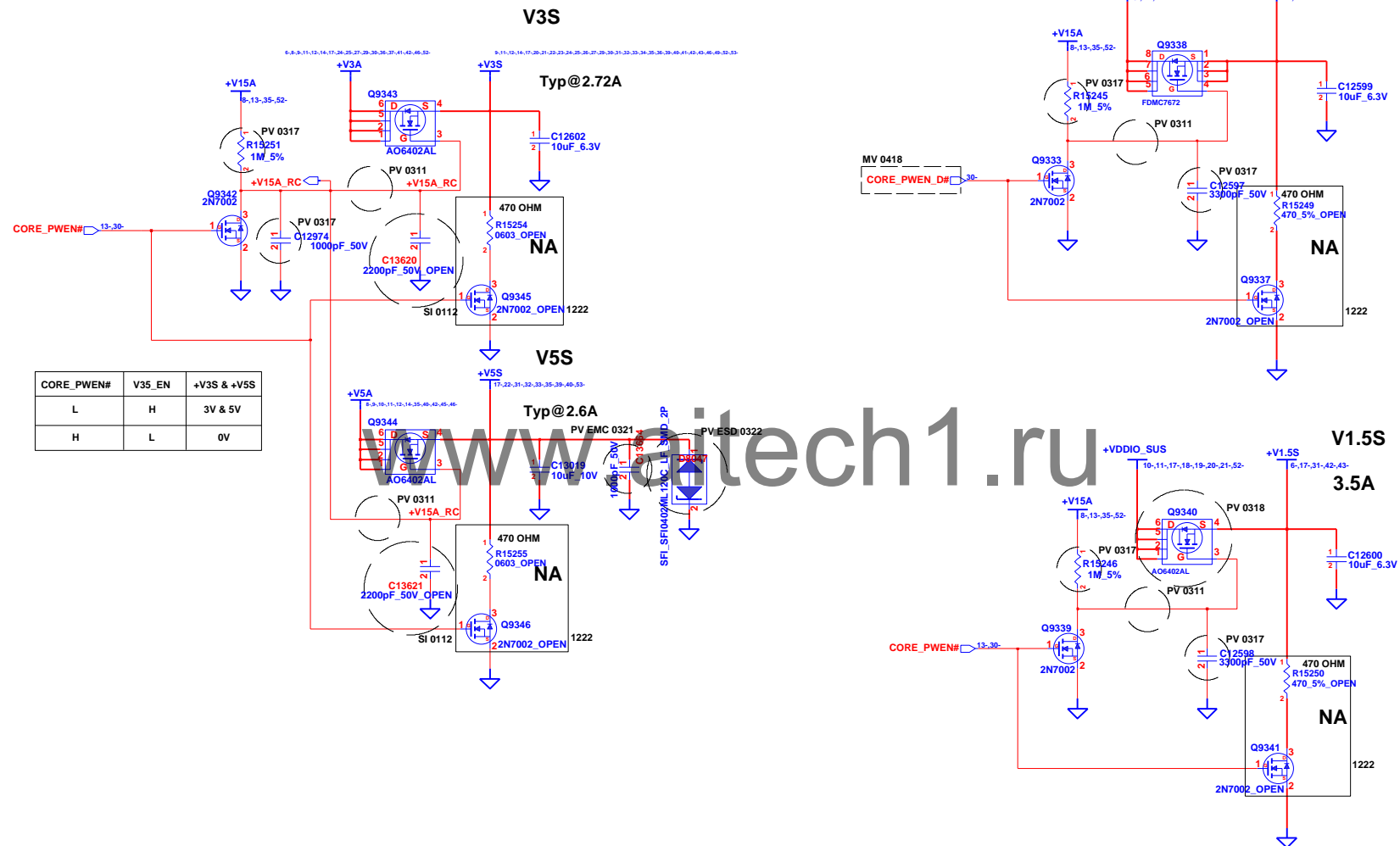
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SIZE A3	CODE CS	DOC. NUMBER 1310A24249-0-MTR	REV A02
SHEET		12	OF 60

CHANGE by	<i>David Cheng</i>	26-Apr-2011
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Q

+V5S & +V3S & +V1.5S & +V1.1S

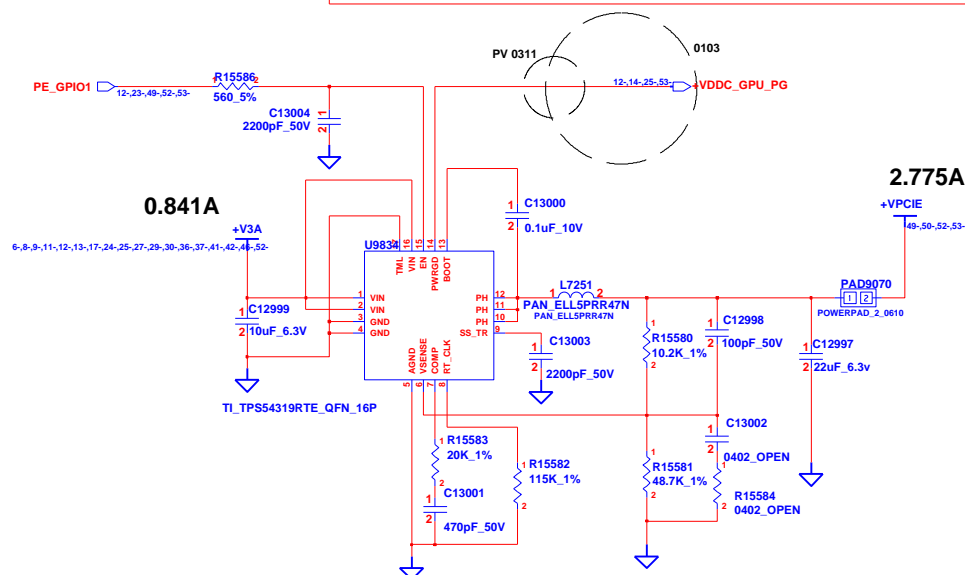
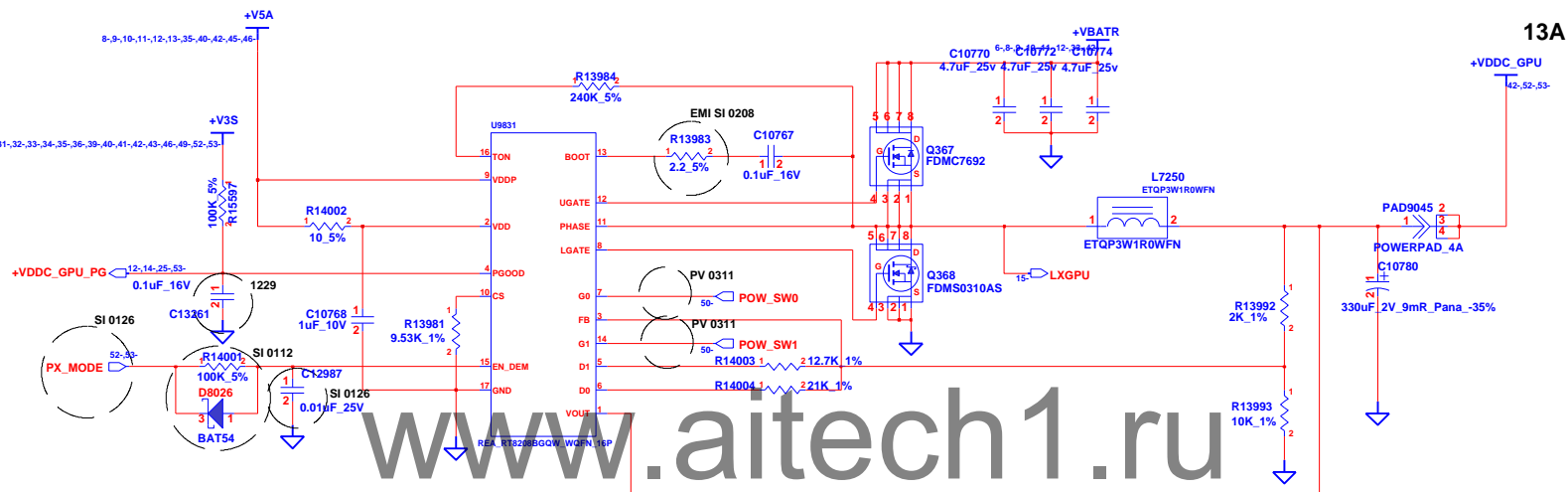


INVENTEC			
TITLE: Hello AMD discrete			
+V5S & +V3S & +V1.5S & +V1.1S			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A24249-0-MTR	REV: A02
CHANGE by: David Cheng		26-Apr-2011	
SHEET: 13		OF: 60	

+VDDC_GPU & +VPCIE

AC-0.8655A
DC-1.522A

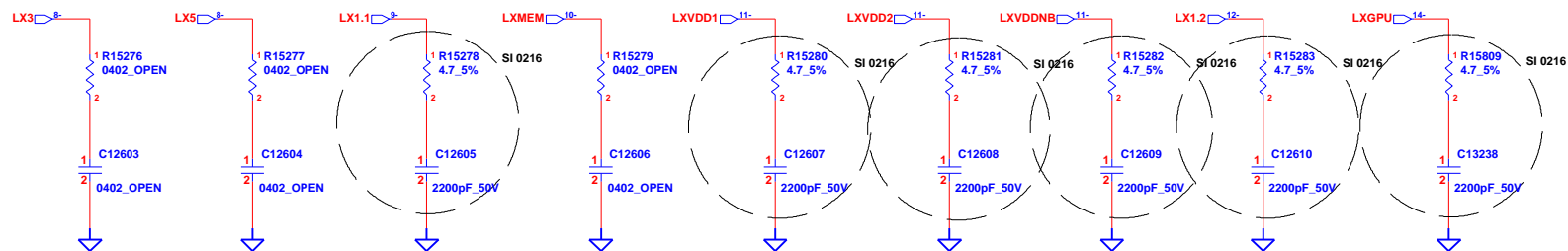
POW_SW1	POW_SW0	+VDDC_GPU	Rtop	Rbot
0	0	1.1V	R50	R55 // R54
0	1	1V	R50	R55
1	0	0.95V	R50 // R91	R55 // R54
1	1	0.9V	R50 // R91	R55



INVENTEC

TITLE			
Hello AMD discrete +VDDC_GPU & +VPCIE			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24249-0-MTR	A02
SHEET		14 OF 60	

CHANGE by David Cheng 26-Apr-2011



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TITLE
Hello AMD discrete

SIZE A3	CODE CS	DOC. NUMBER <i>1310A24249-0-MTR</i>	REV A02
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CHANGE by *David Cheng* 26-Apr-2011

SHEET 15 OF 60

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CHANGE by	<i>David Cheng</i>	<i>26-Apr-2011</i>
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TITLE	<i>Hello AMD discrete GPU</i>
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SIZE A3	CODE CS	DOC. NUMBER 1310A24249-0-MTR	REV A02
SHEET		16	OF 60

CPU

To LVDS ANX3110

To FCH VGA

HDT Header

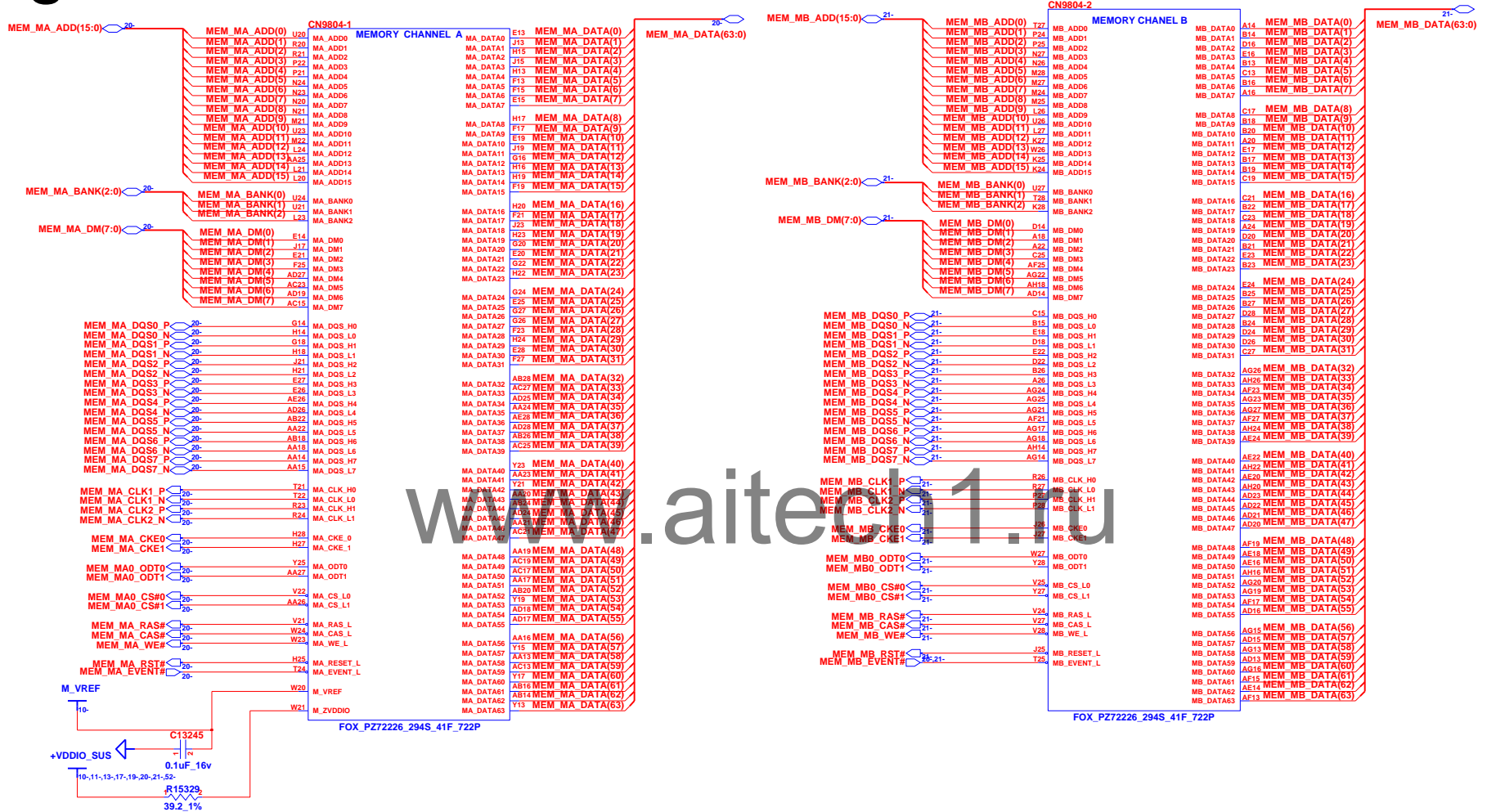
INVENTEC

TITLE	<i>Hello AMD discrete</i>
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SIZE A3	CODE CS	DOC. NUMBER 1310A24249-0-MTR	REV A02
SHEET		17	OF 60

CHANGE by	<i>David Cheng</i>	26-Apr-2011
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CPU

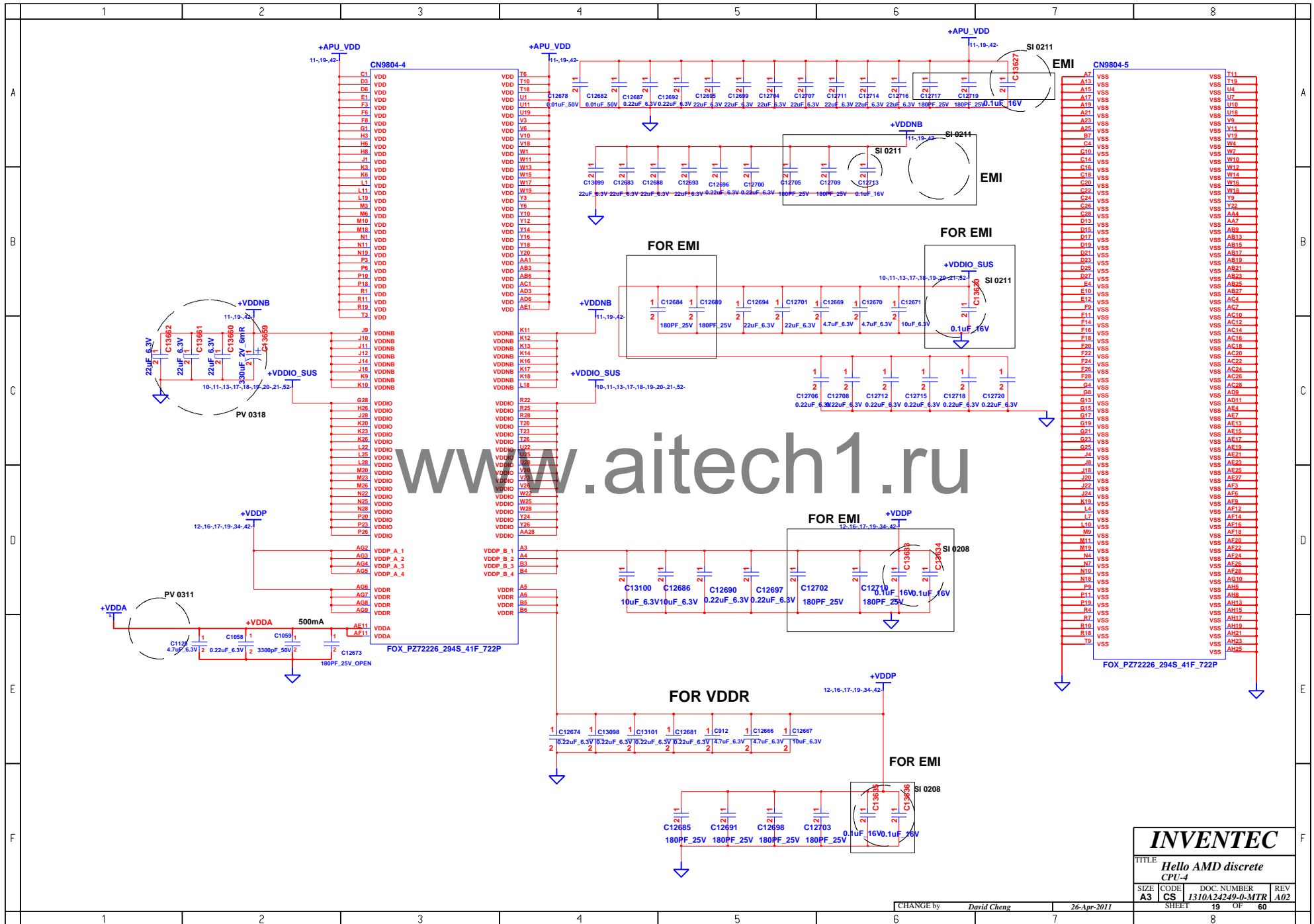


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TITLE Hello AMD discrete CPU-3			
SIZE A3	CODE CS	DOC. NUMBER 1310A24249-0-MTR	REV A02
SHEET 18		OF 60	

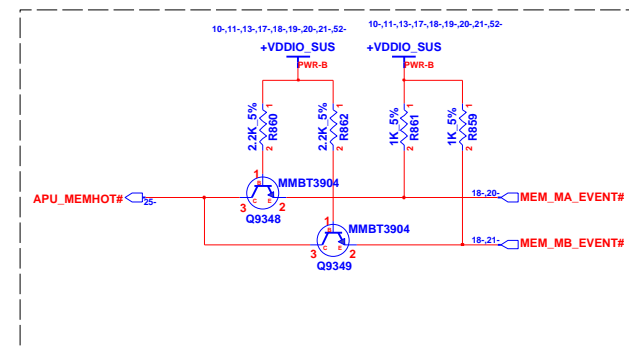
CHANGE by David Cheng 26-Apr-2011

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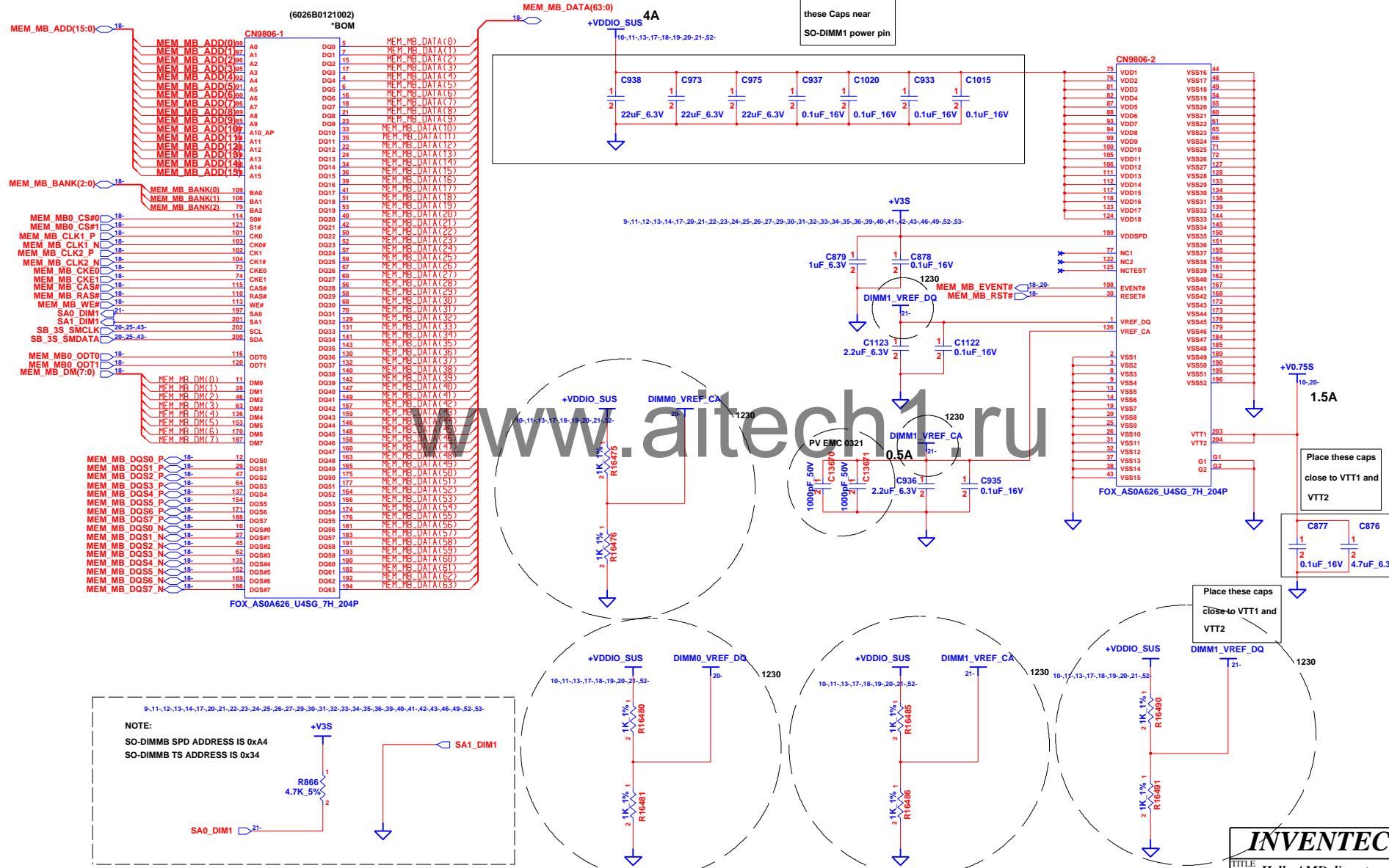
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MEM_MA_ADD(2) 96 A2 D00 9 MEM_MA_DATA(2) SDDR-QQ
MEM_MA_ADD(3) 95 A3 D00 17 MEM_MA_DATA(3) SDDR-QQ
MEM_MA_ADD(4) 94 A4 D00 3 MEM_MA_DATA(4) SDDR-QQ
MEM_MA_ADD(5) 93 A5 D00 8 MEM_MA_DATA(5) SDDR-QQ
MEM_MA_ADD(6) 92 A6 D00 6 MEM_MA_DATA(6) SDDR-QQ
MEM_MA_ADD(7) 91 A7 D00 18 MEM_MA_DATA(7) SDDR-QQ
MEM_MA_ADD(8) 90 A8 D00 21 MEM_MA_DATA(8) SDDR-QQ
MEM_MA_ADD(9) 89 A9 D00 33 MEM_MA_DATA(9) SDDR-QQ
MEM_MA_ADD(10) 88 A10 AP D010 35 MEM_MA_DATA(10) SDDR-QQ
MEM_MA_ADD(11) 87 A11 D010 33 MEM_MA_DATA(11) SDDR-QQ
MEM_MA_ADD(12) 86 A12 D010 24 MEM_MA_DATA(12) SDDR-QQ
MEM_MA_ADD(13) 85 A13 D011 24 MEM_MA_DATA(13) SDDR-QQ
MEM_MA_ADD(14) 84 A14 D011 36 MEM_MA_DATA(14) SDDR-QQ
MEM_MA_ADD(15) 83 A15 D015 36 MEM_MA_DATA(15) SDDR-QQ
MEM_MA_ADD(16) 82 A16 D019 39 MEM_MA_DATA(16) SDDR-QQ
MEM_MA_ADD(17) 81 A17 D017 41 MEM_MA_DATA(17) SDDR-QQ
MEM_MA_ADD(18) 80 A18 D019 53 MEM_MA_DATA(18) SDDR-QQ
MEM_MA_ADD(19) 79 A19 D019 53 MEM_MA_DATA(19) SDDR-QQ
MEM_MA_ADD(20) 78 A20 D020 40 MEM_MA_DATA(20) SDDR-QQ
MEM_MA_ADD(21) 77 A21 D021 40 MEM_MA_DATA(21) SDDR-QQ
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MEM_MA_ADD(28) 70 A28 D026 56 MEM_MA_DATA(28) SDDR-QQ
MEM_MA_ADD(29) 69 A29 D029 68 MEM_MA_DATA(29) SDDR-QQ
MEM_MA_ADD(30) 68 A30 D030 70 MEM_MA_DATA(30) SDDR-QQ
MEM_MA_ADD(31) 67 A31 D032 129 MEM_MA_DATA(31) SDDR-QQ
MEM_MA_ADD(32) 66 A32 D033 141 MEM_MA_DATA(32) SDDR-QQ
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MEM_MA_ADD(35) 63 A35 D036 130 MEM_MA_DATA(35) SDDR-QQ
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MEM_MA_ADD(124) 0 A124 D057 187 MEM_MA_DATA(
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INVENTEC			
TITLE <i>Hello AMD discrete SO-DIMM0</i>			
SIZE A3	CODE CS	DOC. NUMBER <i>1310A24249-0-MTR</i>	R <i>A</i>
SHEET		20 OF	60

SO-DIMM1-ST_400

Layout Note: Place
these Caps near
SO-DIMM1 power pin



INVENTEC

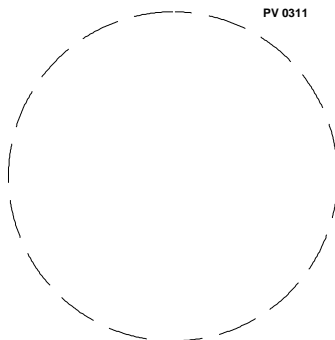
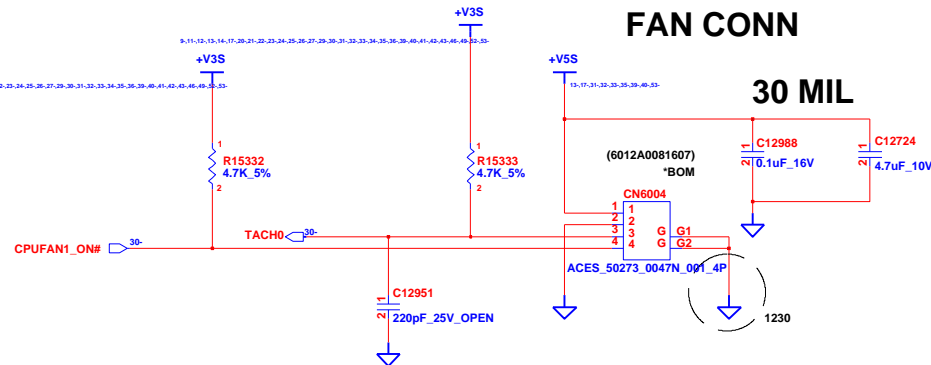
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Hello AMD discrete
SO-DIMM1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24249-0-MTR	A02

CHANGE by David Cheng 26-Apr-2011

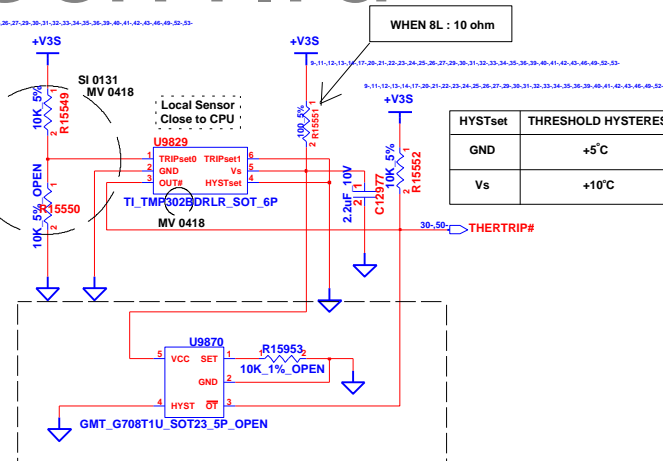
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TRIPset1	TRIPset0	TMP302C
GND	GND	+90°C
GND	Vs	+95°C
Vs	GND	+100°C
Vs	Vs	+105°C

TRIPset1	TRIPset0	TMP302C
GND	GND	+70°C
GND	Vs	+75°C
Vs	GND	+80°C
Vs	Vs	+85°C



HYSTset	THRESHOLD HYSTERESIS
GND	+5°C
Vs	+10°C

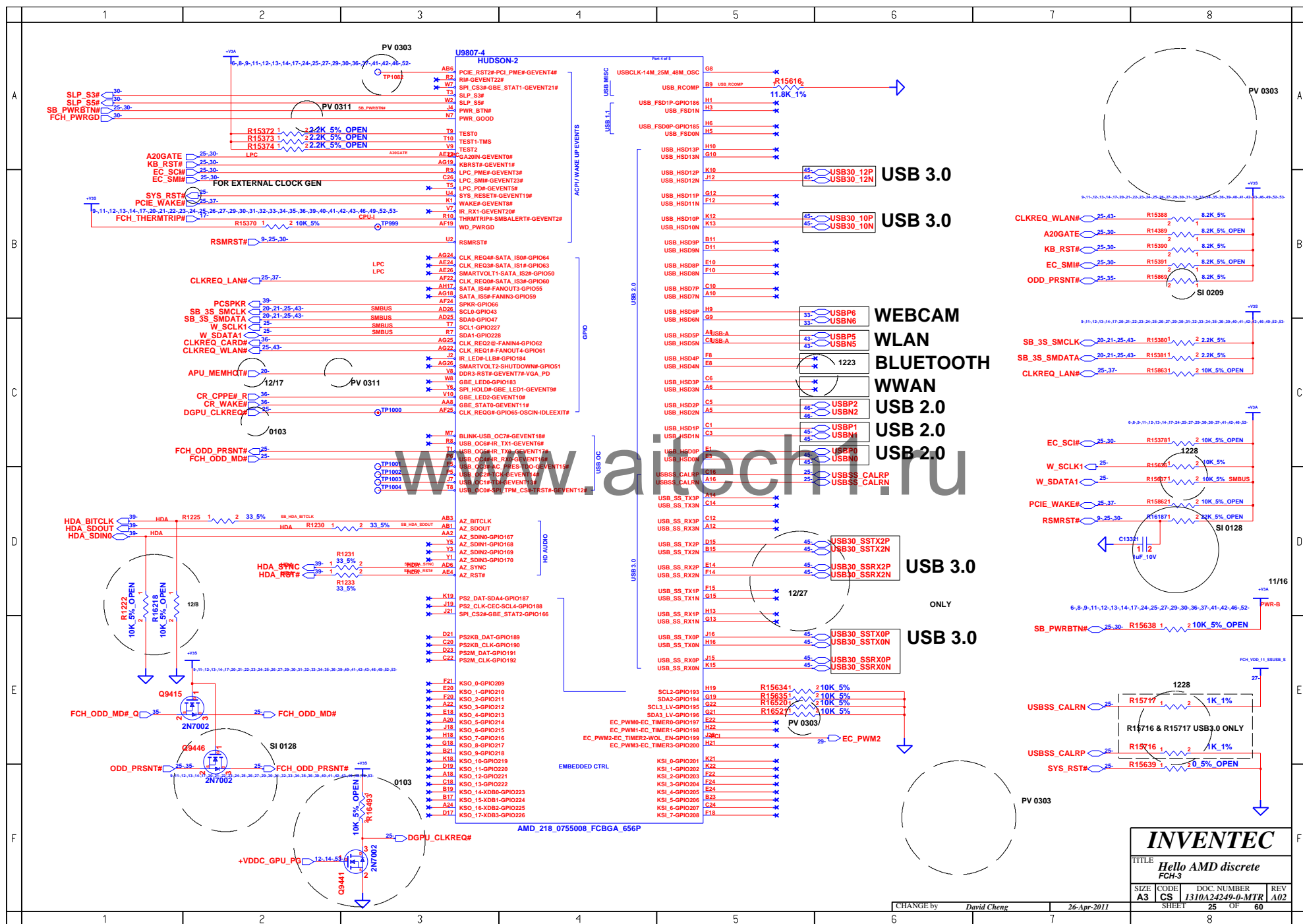
INVENTEC

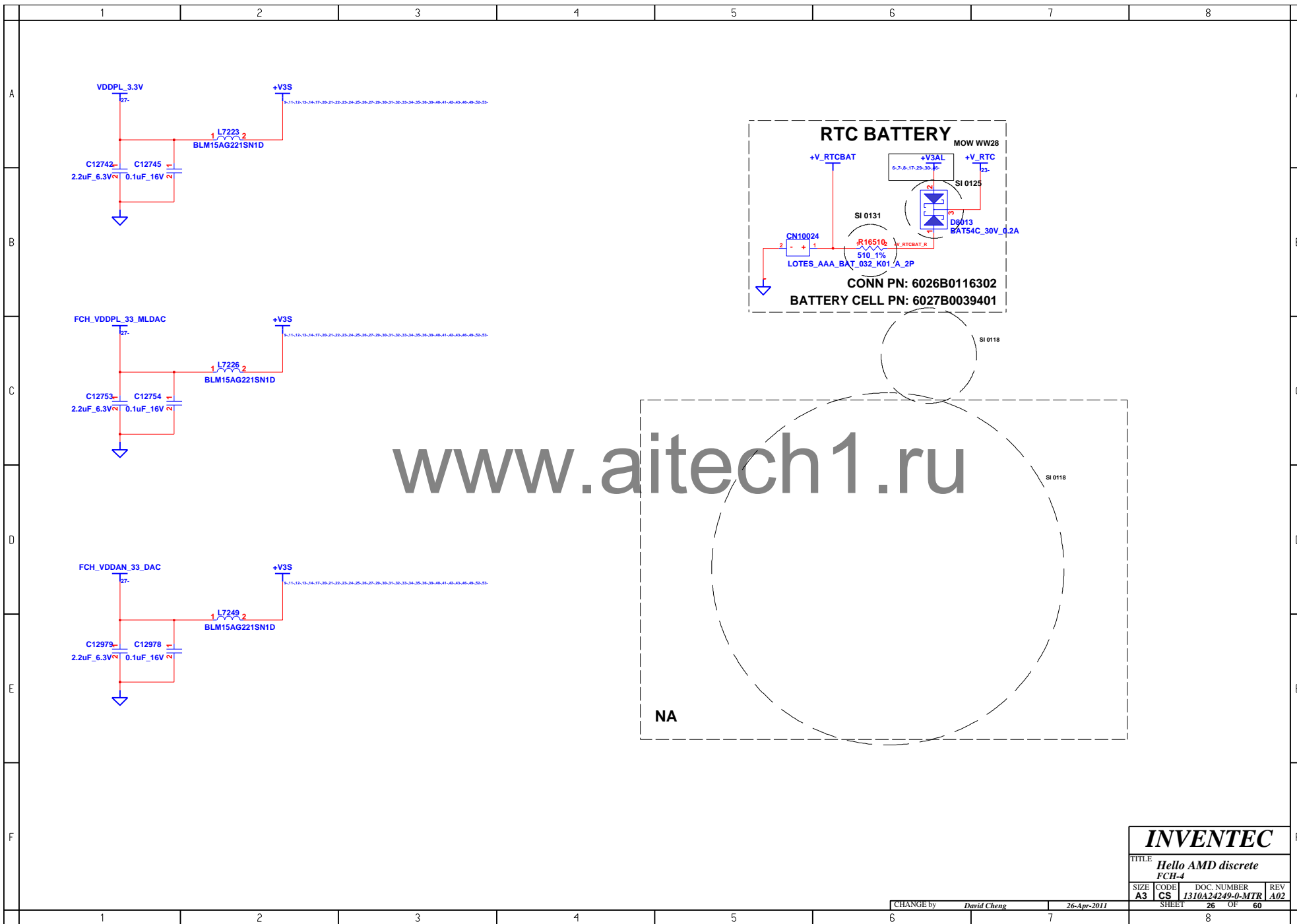
TITLE
Hello AMD discrete
FAN & THERMAL IC

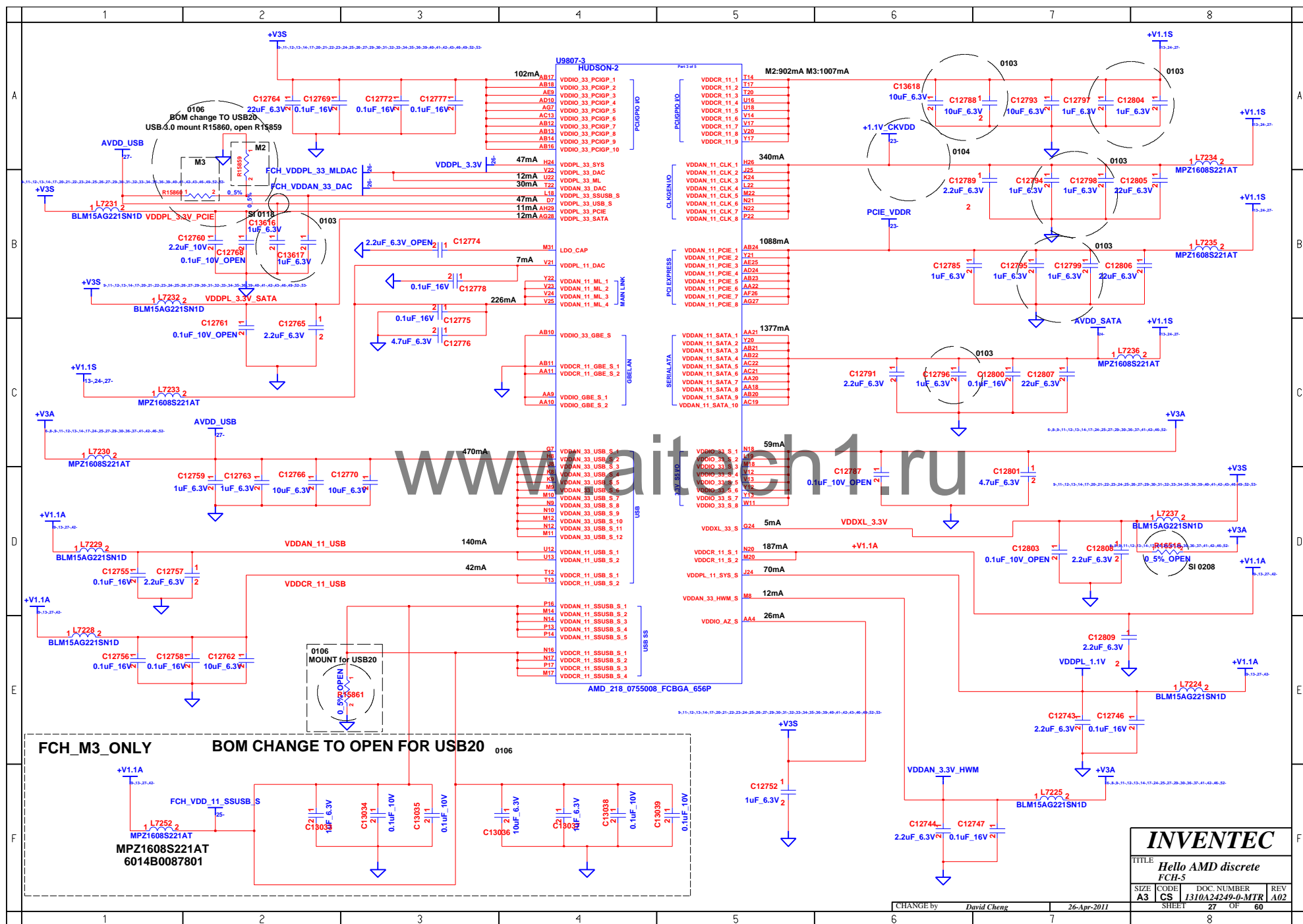
SIZE A3	CODE CS	DOC. NUMBER 1310A24249-0-MTR	REV A02
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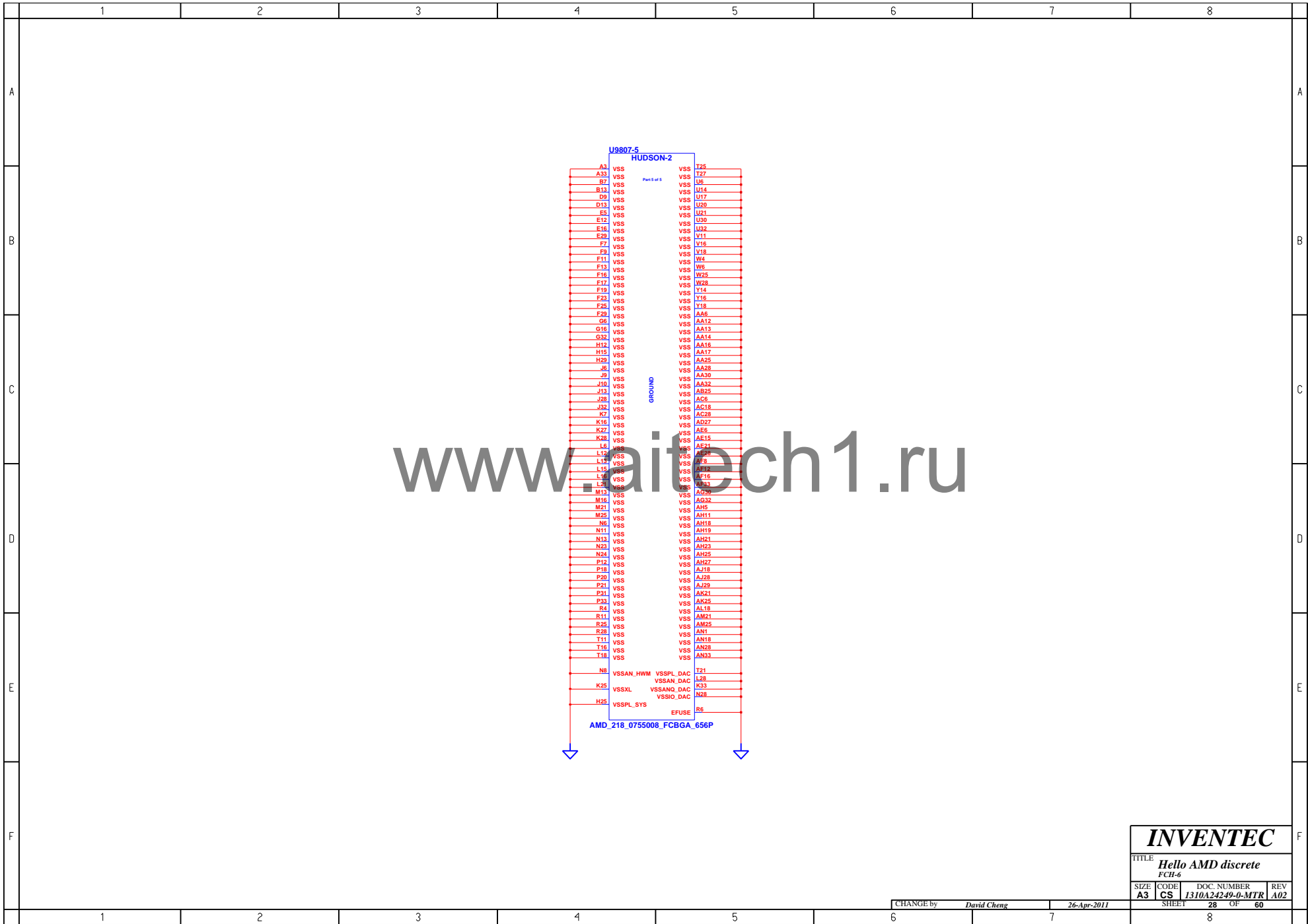
CHANGE by David Cheng 26-Apr-2011

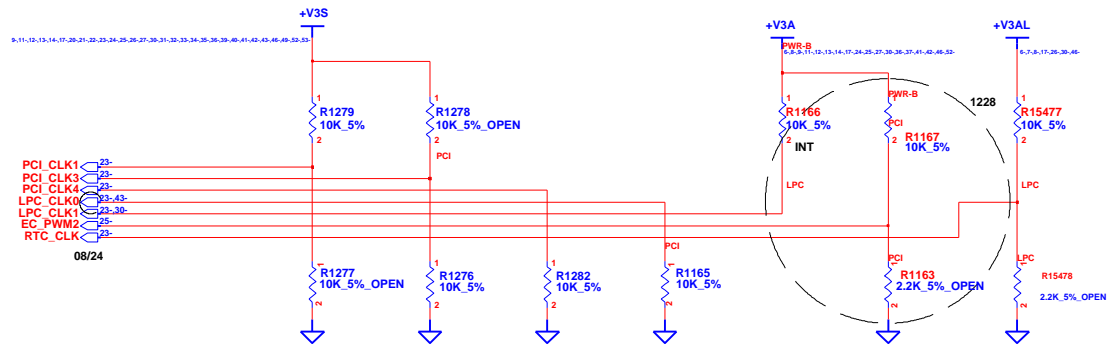
SHEET 22 OF 60







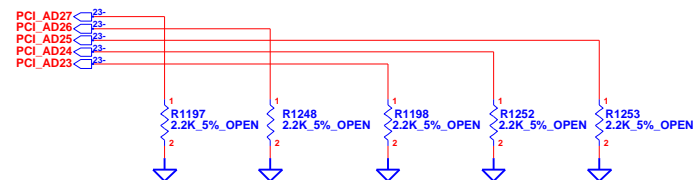




Required Straps:

RTCCCLK		PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	PCI_CLK1	EC_PWM2
S5 PLUS MODE DISABLE (DEFAULT)	PULL HIGH	ALLOW PCIE Gen2 DEFAULT	USE DEBUG STRAP	non Fusion CLOCK MODE DEFAULT APU_CLK AND DISP_CLK NO CLOCK OUTPUT	EC ENABLED	INTEGRATED CLKGEN ENABLED DEFAULT	LPC ROM
S5 PLUS MODE ENABLE	PULL LOW	FORCE PCIE Gen1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK MODE DEFAULT APU_CLK AND DISP_CLK CLOCK OUTPUT FROM INT CLOCK GEN	EC DISABLED DEFAULT	INTEGRATED CLKGEN DISABLED	SPI ROM DEFAULT

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Debug Straps

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (default)	DISABLE ILA AUTORUN (default)	USE FC PLL (default)	USE DEFAULT PCIE STRAPS (default)	DISABLE PCI MEM BOOT (default)
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PCI PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

INVENTEC

TITLE
**Hello AMD discrete
STRAP**

SIZE A3	CODE CS	DOC. NUMBER 1310A24249-0-MTR	REV A02
SHEET 29		OF 60	

CHANGE by *David Cheng* 26-Apr-2011

KBC

	DIS 90W	UMA 65W
MB_ID2	0	1
PU	0	1
PD	0	1

	DB	SI	PV	MV
MB_ID0	0	1	0	1
MB_ID1	0	0	1	1

BOARD ID

INVENTEC

TITLE
Hello AMD discrete
KBC

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24249-0-MTR	A02
SHEET	30	OF	60

CHANGE by **David Cheng** 26-Apr-2011

HDMI

TITLE			
<i>Hello AMD discrete</i> <i>HDMI</i>			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24249-0-MTR	A02
SHEET		31	OF 60

CHANGE by	<i>David Cheng</i>	26-Apr-2011
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LVDS

LVDS

[illegible]

LVDS

LVDS

[illegible][illegible][illegible]

A



C

D

E

F

A

22

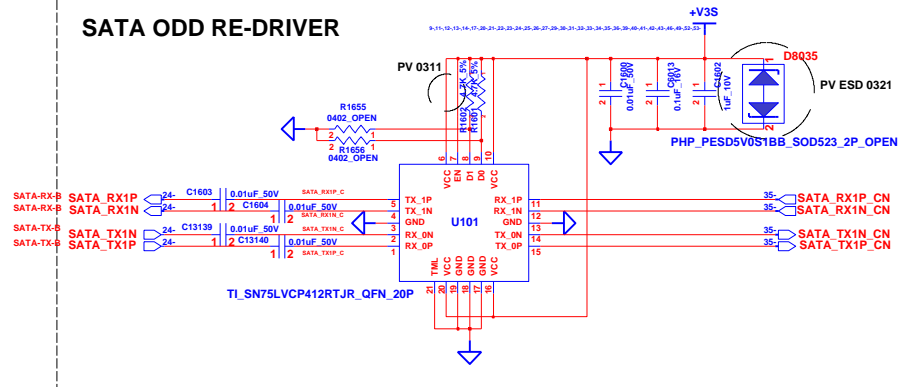
C

0

E

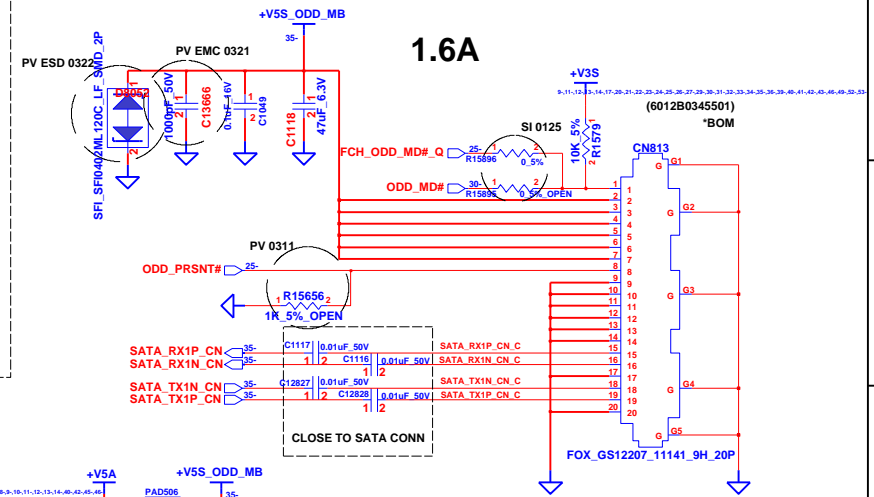
F

SATA ODD RE-DRIVER



SATA ODD CONN

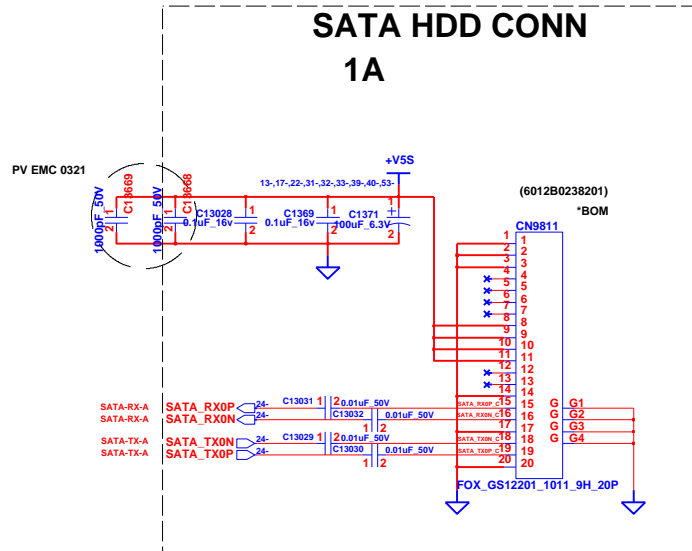
1.6A



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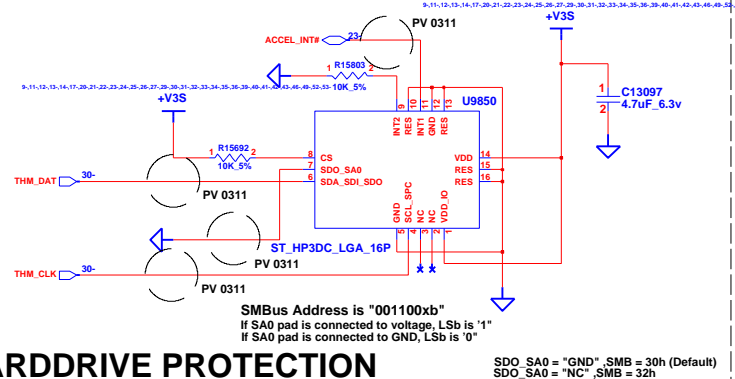
SATA HDD CONN

1A



HARDDRIVE PROTECTION

P/N = 6019B0800501

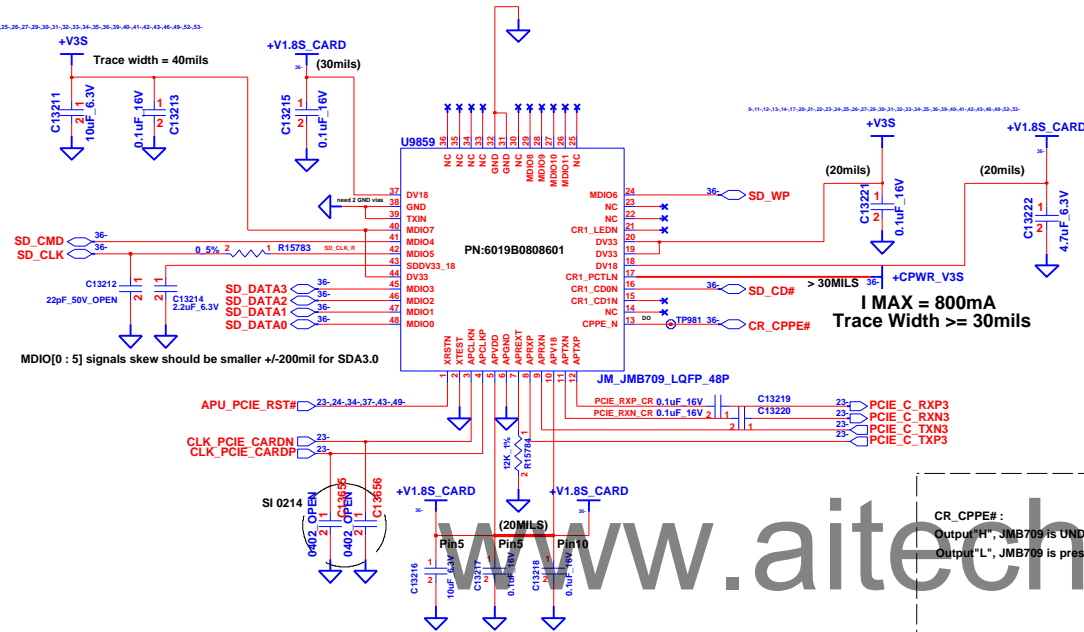


INVENTEC

TITLE			
Hello AMD discrete			
SATA HDD & ODD CONN			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A24249-0-MTR	A02
SHEET		35	OF 60

CHANGE by David Cheng 26-Apr-2011

Card Reader - JMB709

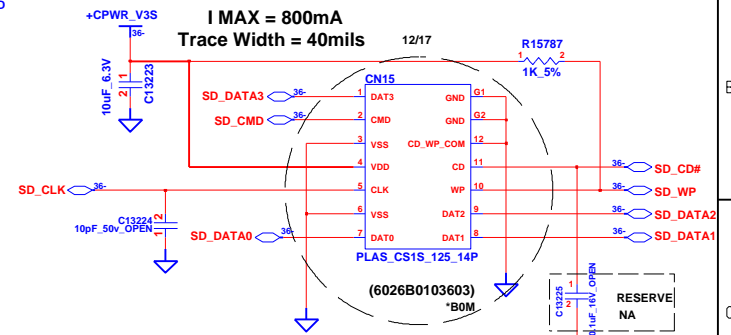


Layout Note :

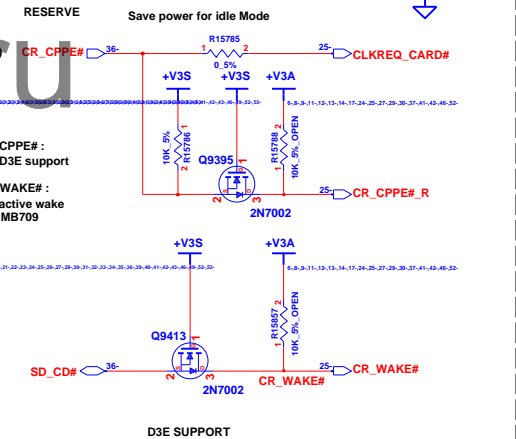
- C13217 CLOSE TO PIN5 (Trace width/length : 11mils/<100mils)
- C13216 Close to C13217 (Trace width/length : 20mils/<40mils)
- C13218 close to pin10 (Trace width/length : 11mils/<100mils)
- APREXT trace width/length : 12mils/<250mils
- C13222 close to pin18 (Trace width/length : 12mils/<100mils for internal REG)

Without card	CD —○—○— CD / WP Com
	WP —○—○— CD / WP Com
Inserted card(unlock)	CD —○—○— CD / WP Com
	WP —○—○— CD / WP Com
Inserted card(lock)	CD —○—○— CD / WP Com
	WP —○—○— CD / WP Com

Card Reader CONN



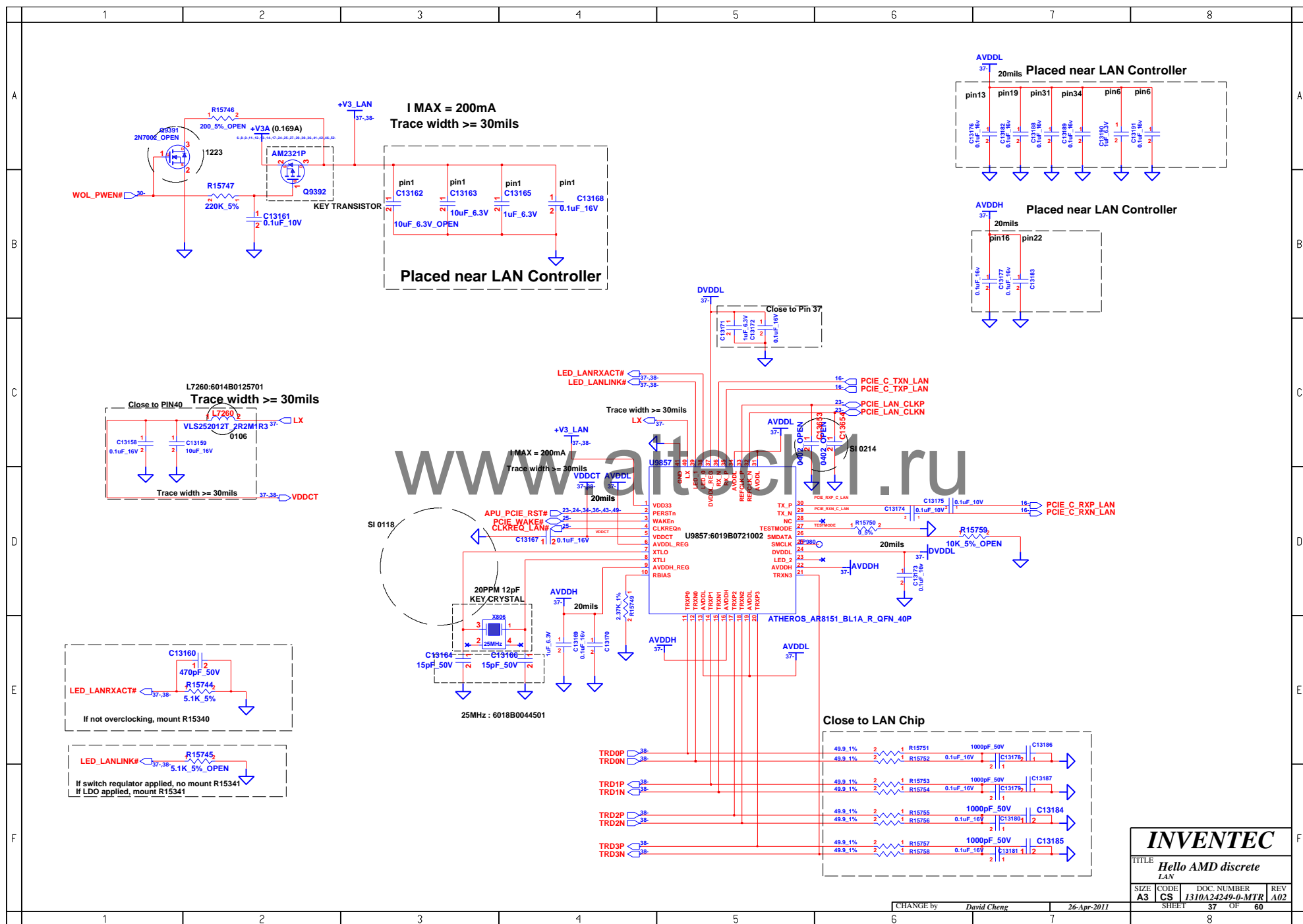
CR_CPPE# :
Output "H", JMB709 is UNDER D3E mode (disappear)
Output "L", JMB709 is present, non D3E mode



INVENTEC

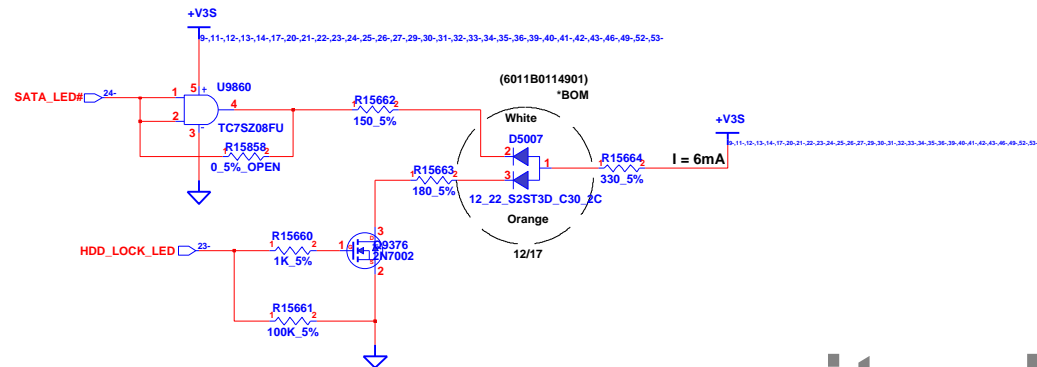
TITLE Hello AMD discrete CARD READER-JMB709			
SIZE A3	CODE CS	DOC. NUMBER 1310A24249-0-MTR	REV A02
SHEET 36		OF 60	

CHANGE by David Cheng 26-Apr-2011

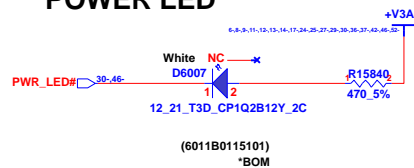


SATA LED & POWER LED

SATA LED & HDD-HALTED LED



POWER LED



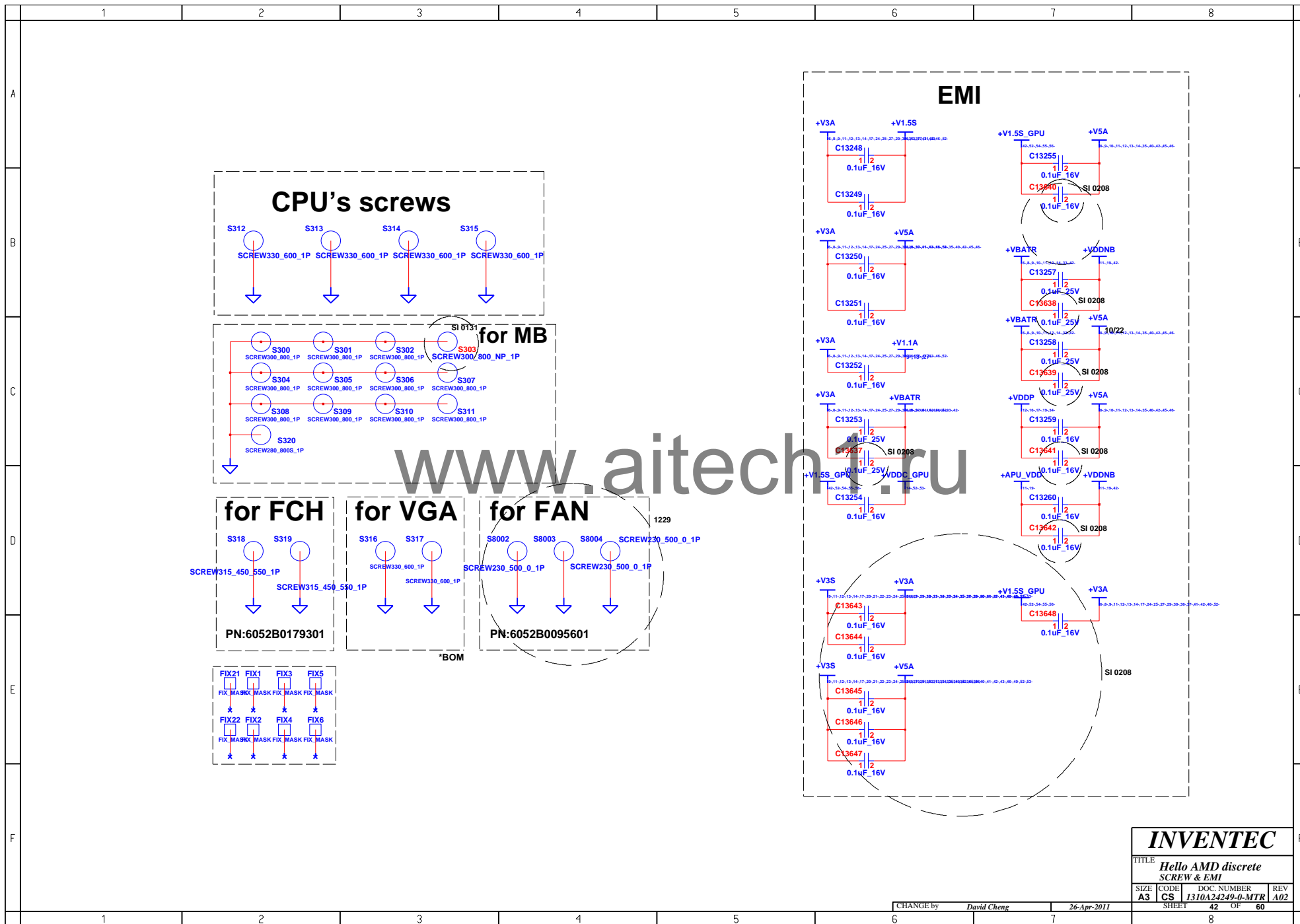
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INVENTEC

TITLE			
Hello AMD discrete SATA LED & PWR LED			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24249-0-MTR	A02
SHEET		41	OF 60

CHANGE by David Cheng 26-Apr-2011

8

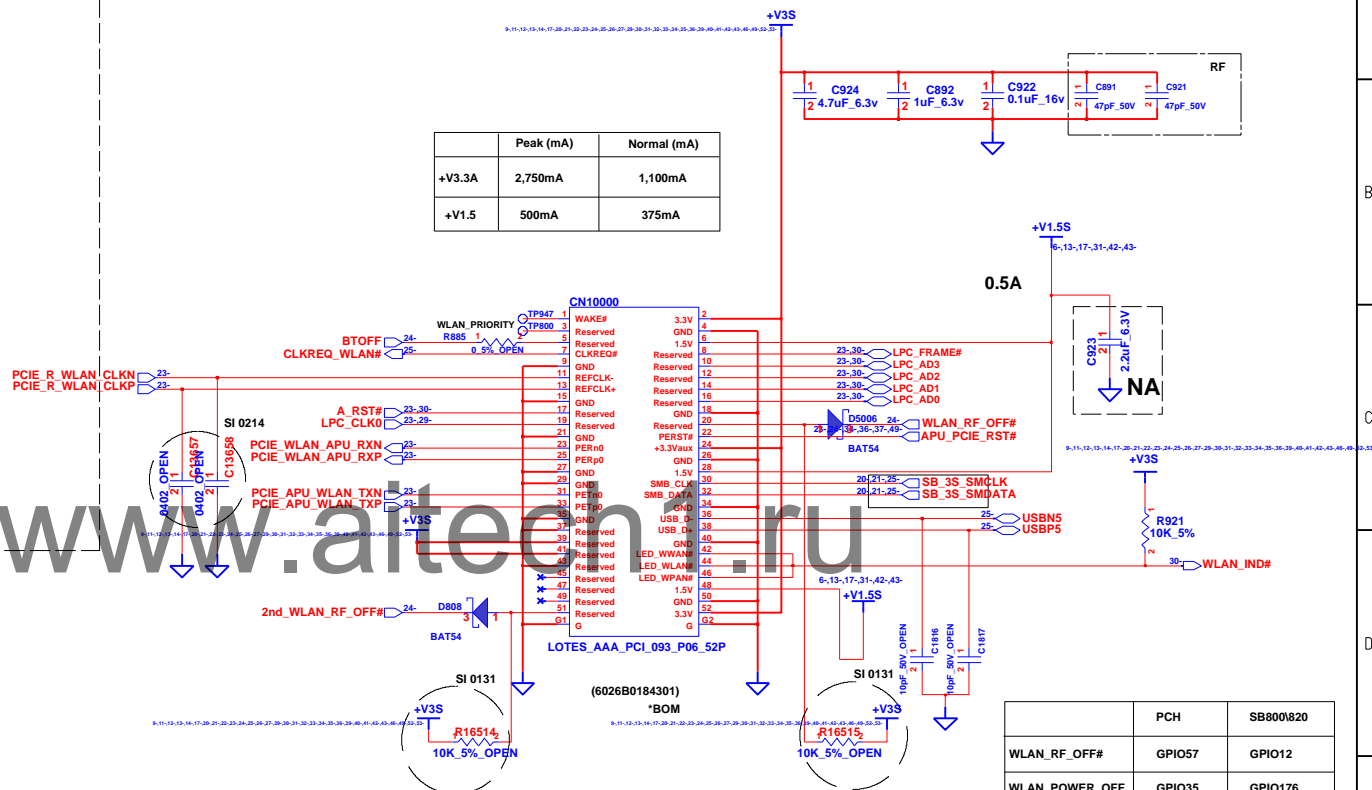


BLUETOOTH CONN

NA

WLAN CONN (MINICARD)

	Peak (mA)	Normal (mA)
+V3.3A	2,750mA	1,100mA
+V1.5	500mA	375mA



	PCH	SB800/820
WLAN_RF_OFF#	GPIO57	GPIO12
WLAN_POWER_OFF	GPIO35	GPIO176

INVENTEC

TITLE
Hello AMD discrete
WLAN & BT

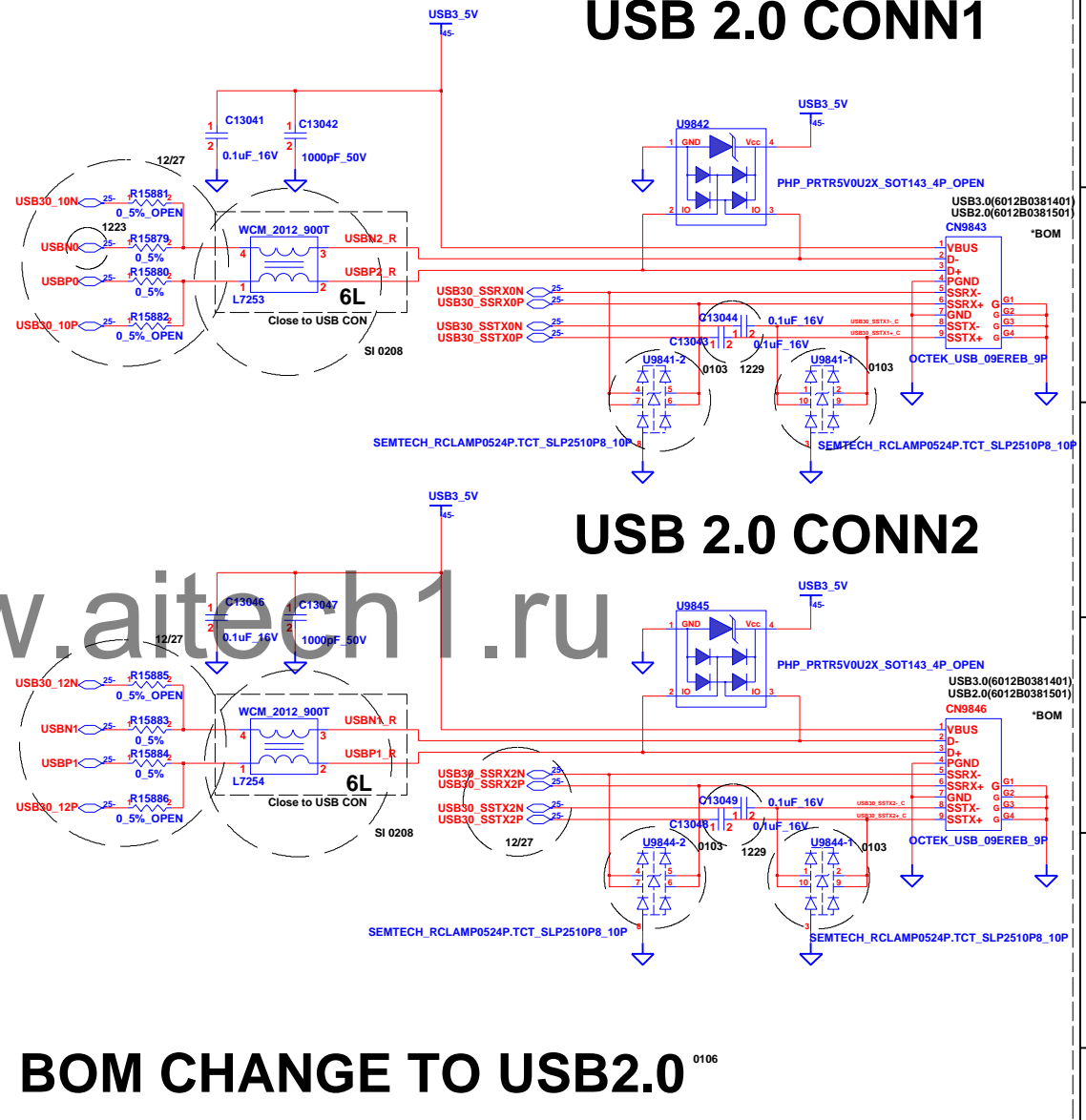
SIZE CODE DOC. NUMBER REV
A3 CS 1310A24249-0-MTR A02

CHANGE by David Cheng 26-Apr-2011

SHEET 43 OF 60

	1	2	3	4	5	6	7	8	
A	<div>NA</div> <div>www.aitech1.ru</div>								A
B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

INVENTEC			
TITLE Hello AMD discrete WWAN & SIM CARD			
SIZE A3	CODE CS	DOC. NUMBER 1310A24249-0-MTR	REV A02
CHANGE by David Cheng		26-Apr-2011	
SHEET 44		OF 60	



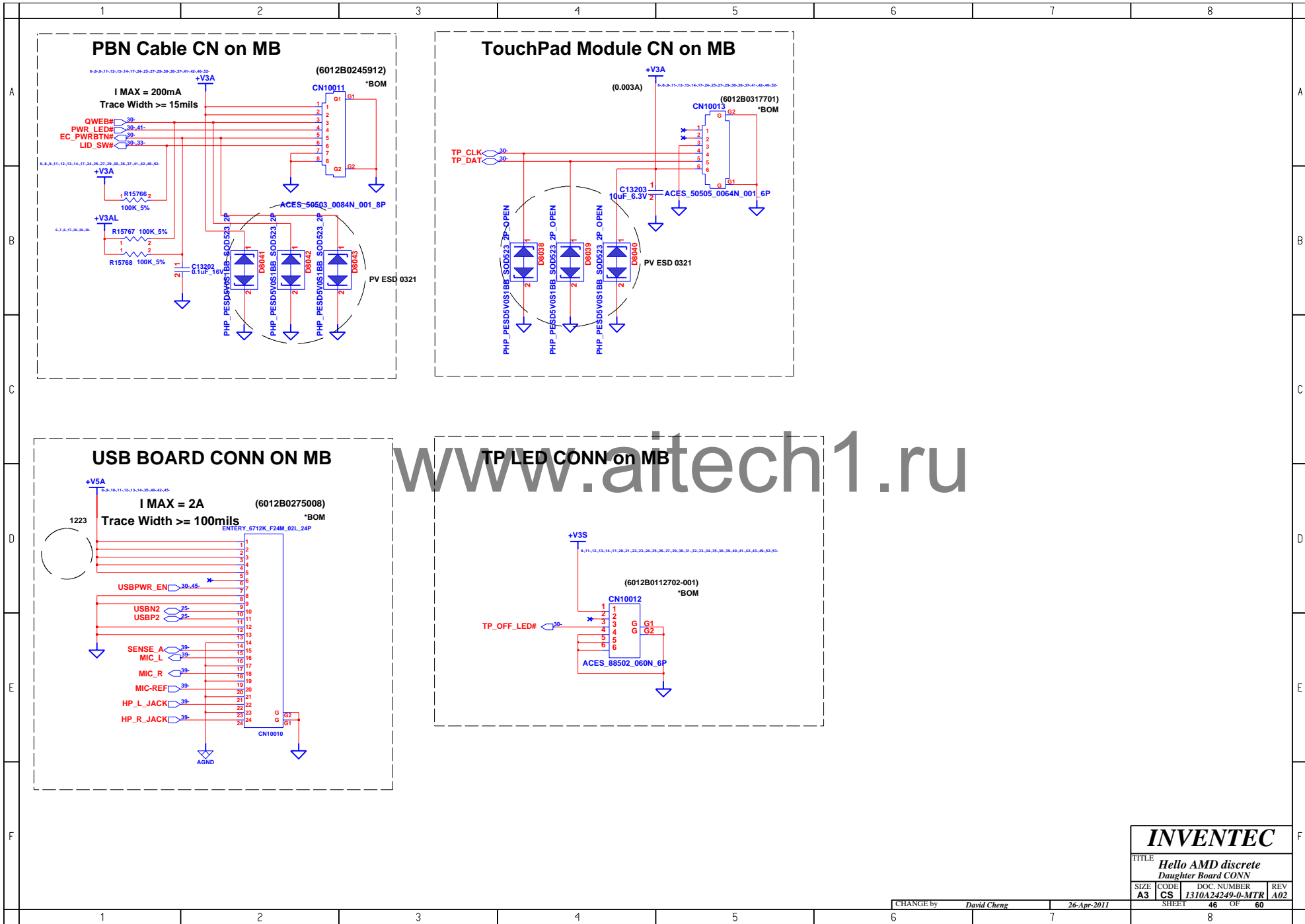
BOM CHANGE TO USB2.0 ⁰¹⁰⁶

INVENTEC

TITLE *Hello AMD discrete
USB 3.0 CONN*

SIZE A3	CODE CS	DOC. NUMBER 1310A24249-0-MTR	REV A02
SHEET		45	OF 60

CHANGE by	<i>David Cheng</i>	26-Apr-2011
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INVENTEC

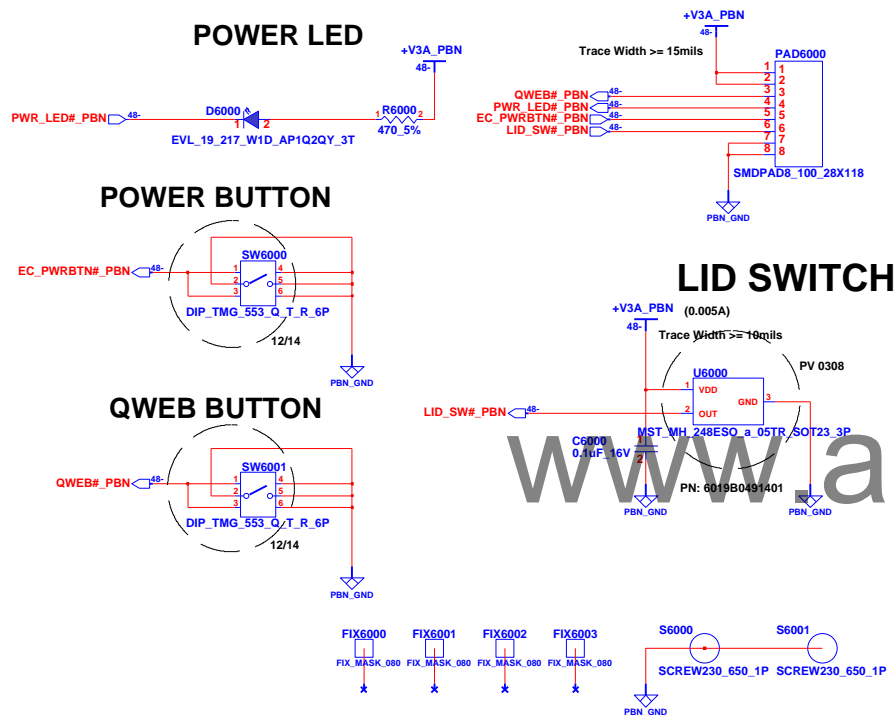
TITLE
**Hello AMD discrete
Daughter Board CONN**

SIZE A3	CODE CS	DOC. NUMBER 1310A24249-0-MTR	REV A02
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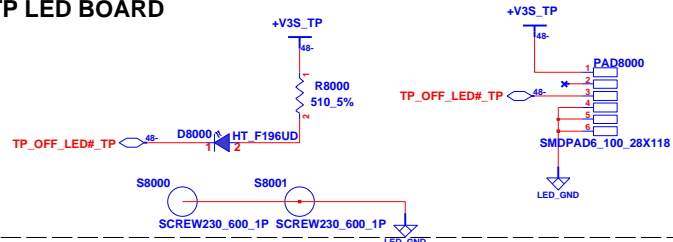
CHANGE by **David Cheng** 26-Apr-2011

SHEET **46** OF **60**

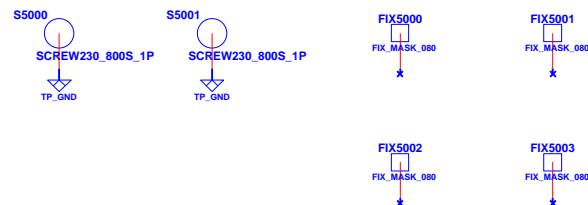
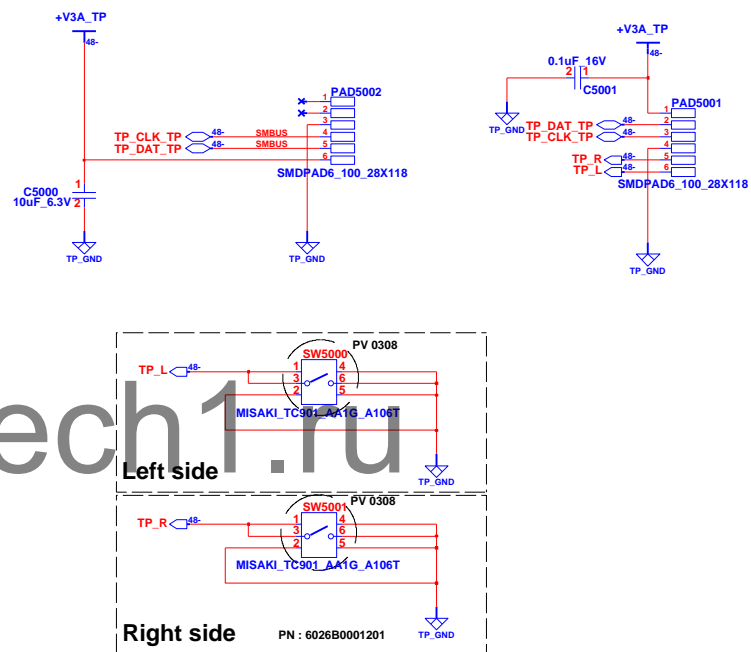
POWER BOTTON BOARD



TP LED BOARD



PICK BUTTON BOARD



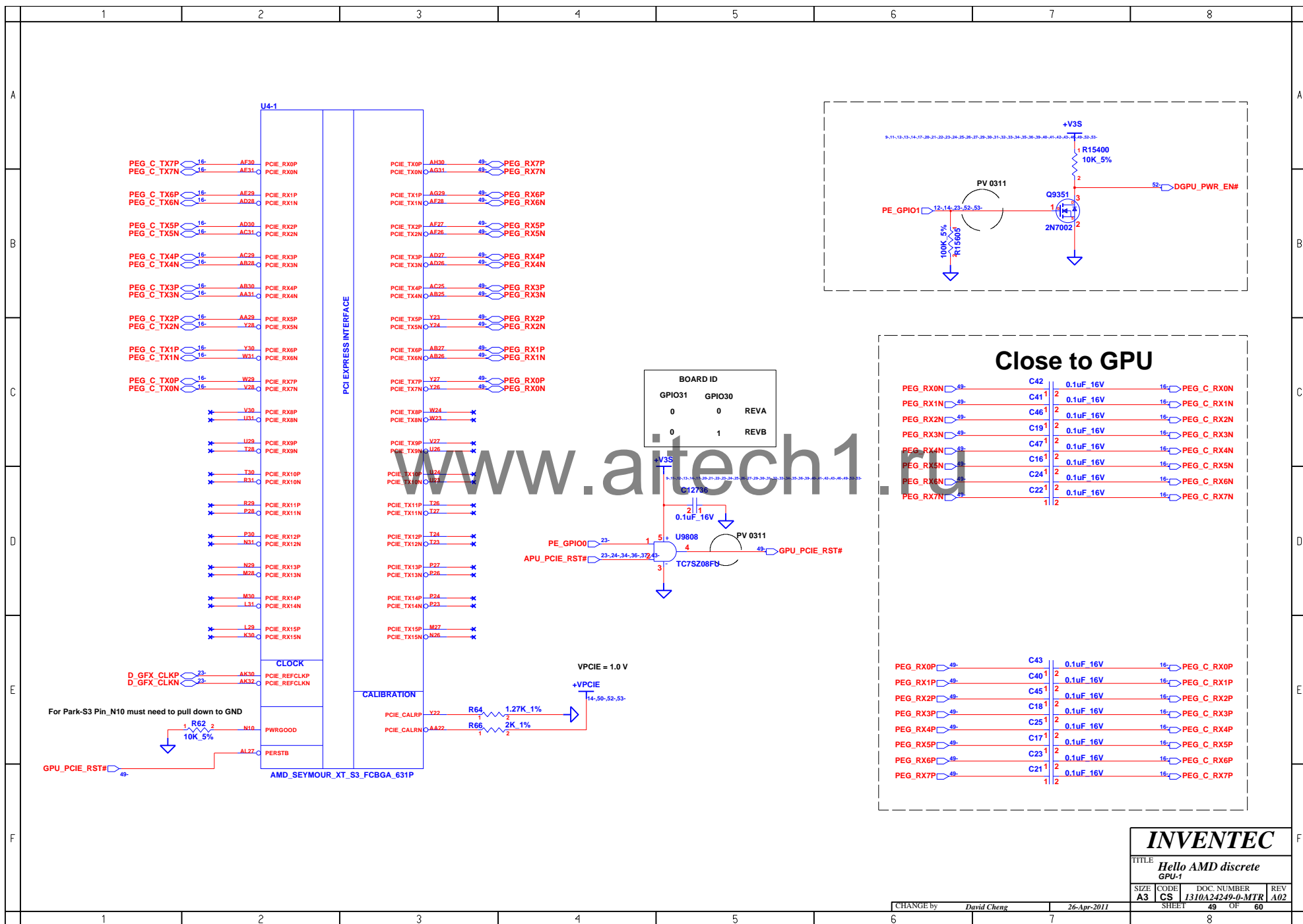
INVENTEC

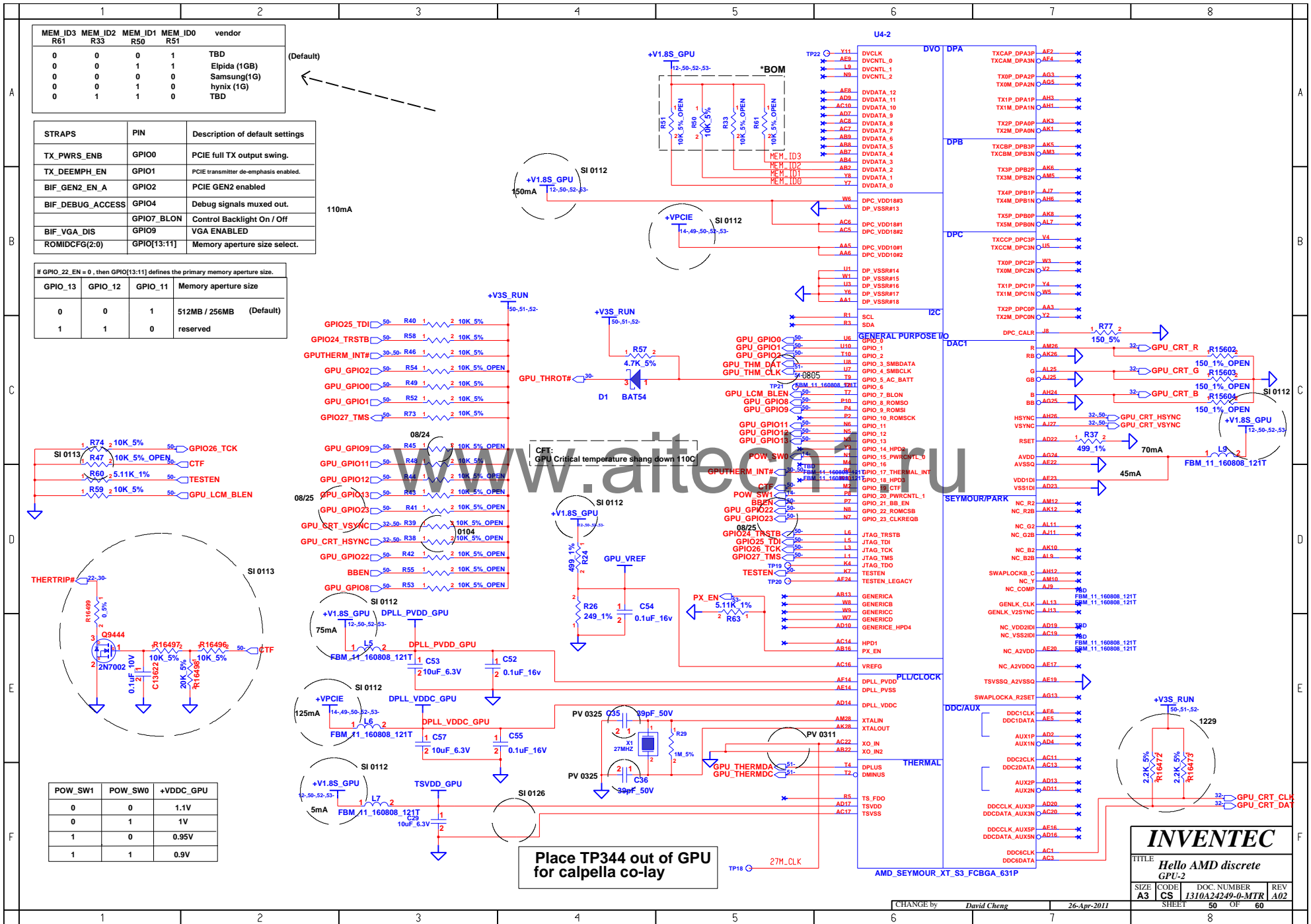
TITLE: Hello AMD discrete

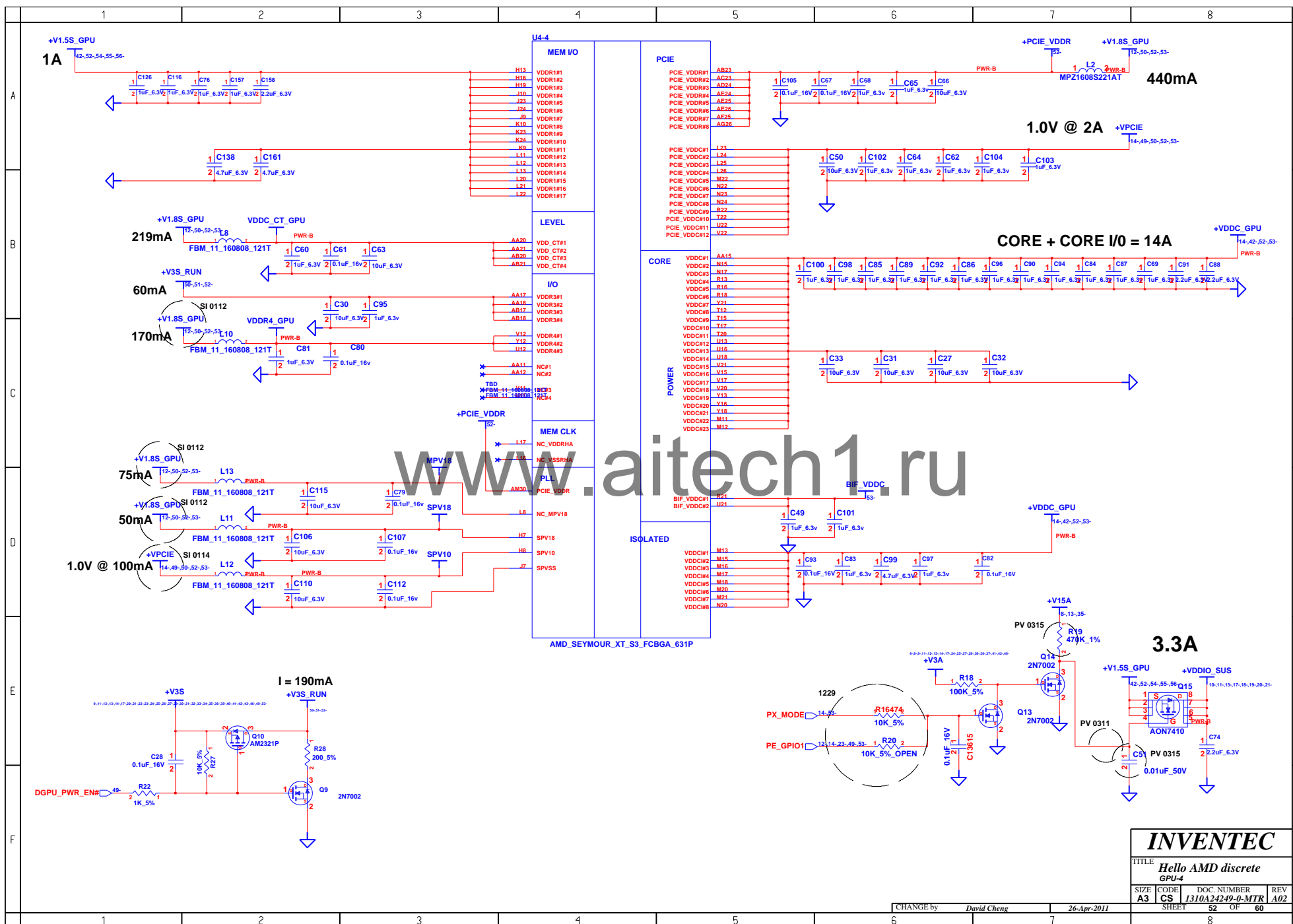
SIZE: A3
CODE: CS
DOC. NUMBER: 1310A24249-0-MTR
REV: A02

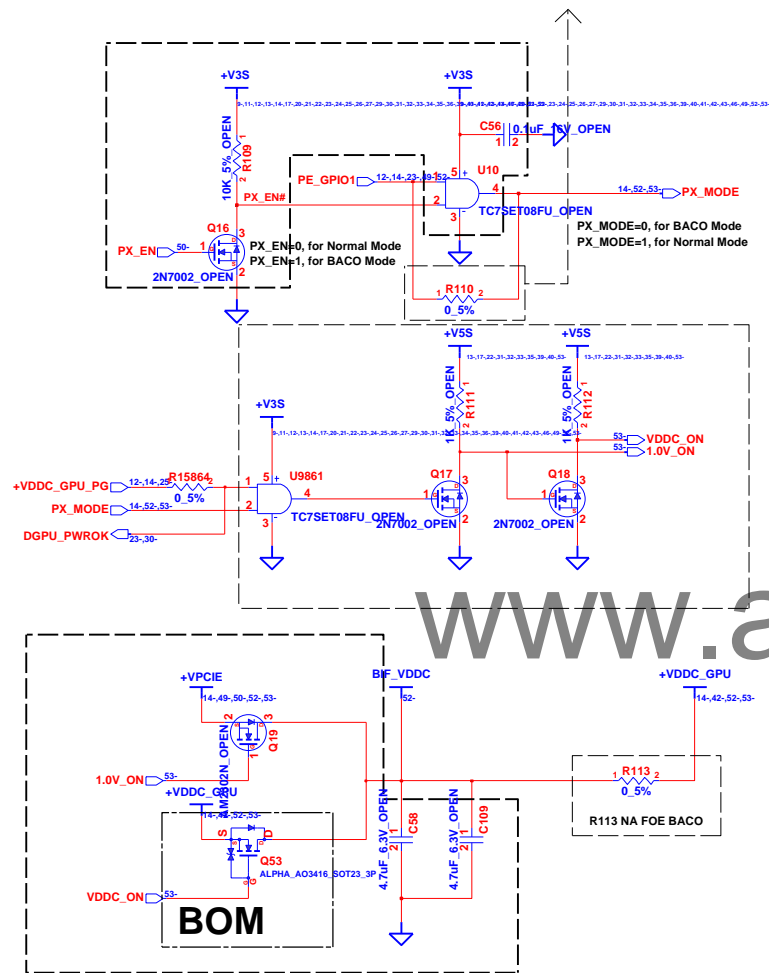
CHANGE by: David Cheng 26-Apr-2011

SHEET 48 OF 60





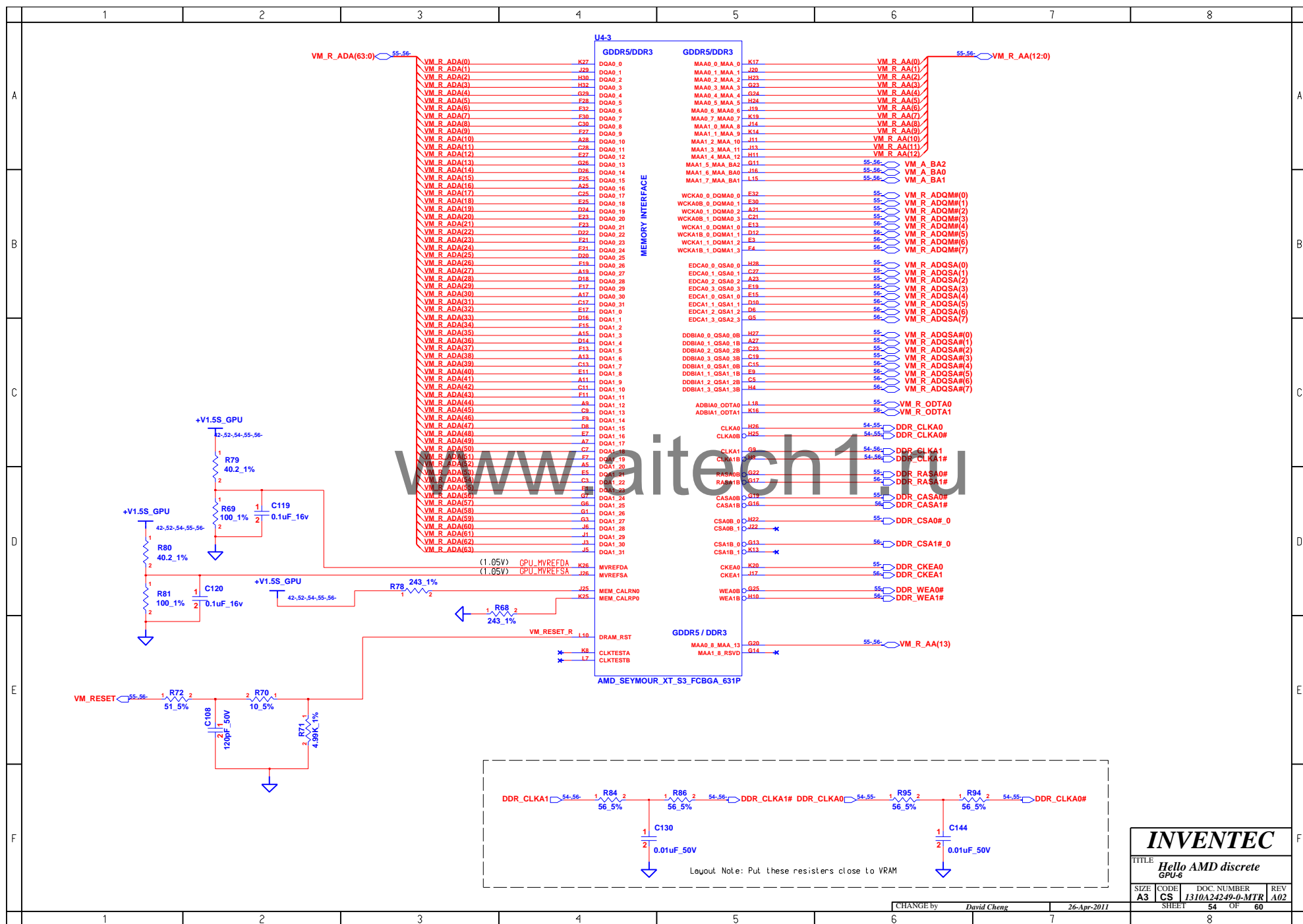


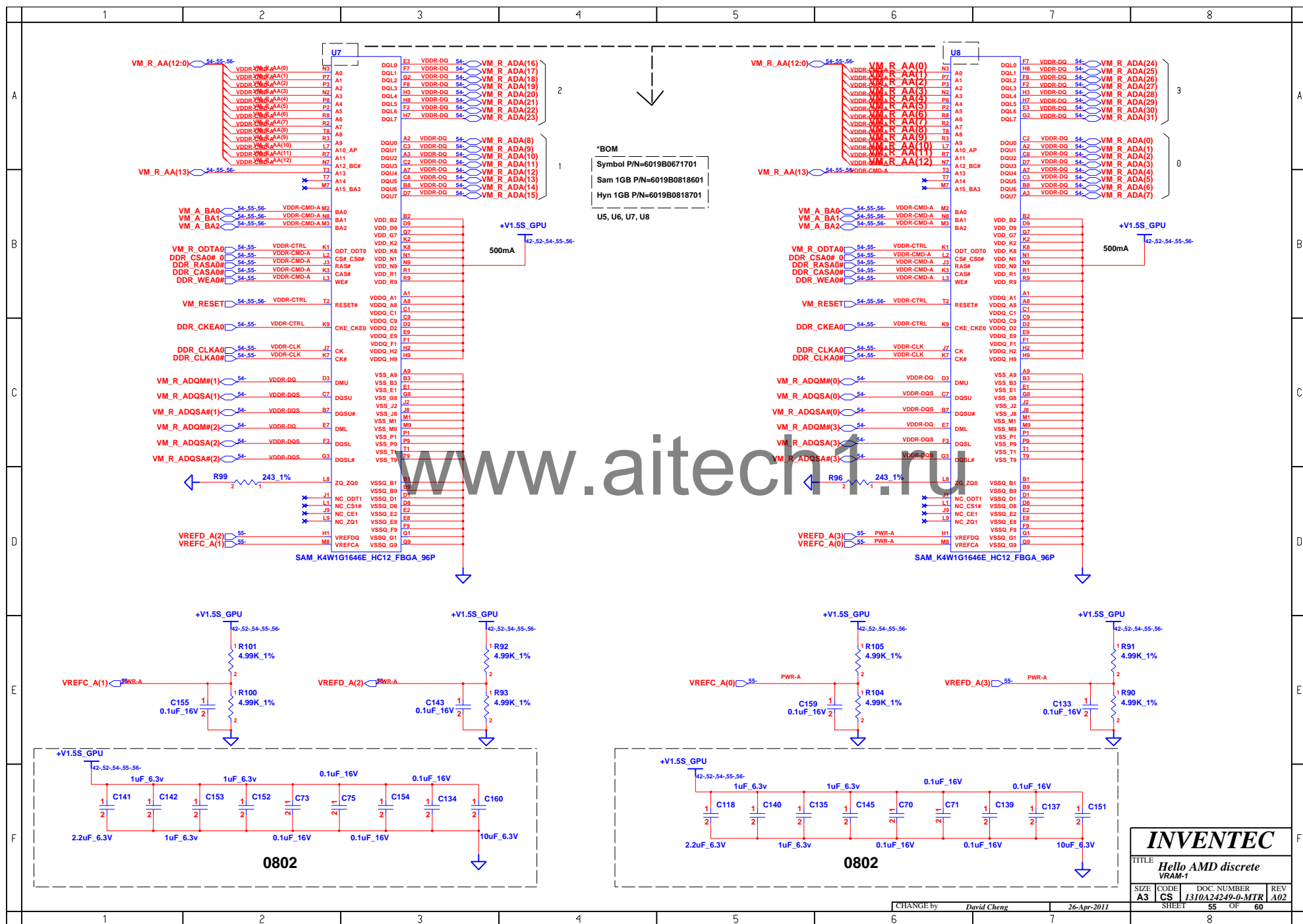


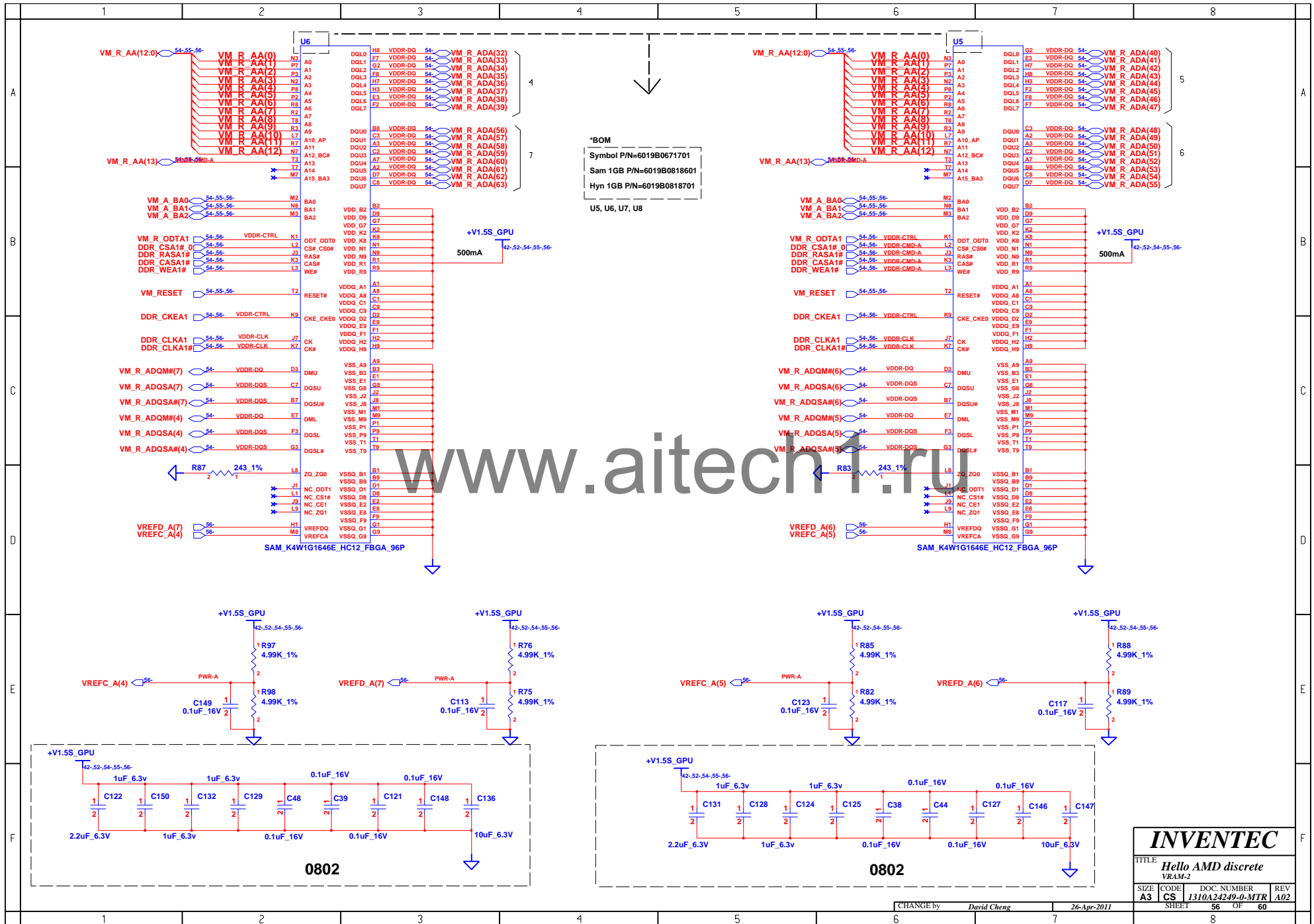
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TITLE			
<i>Hello AMD discrete GPU-5</i>			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	<i>1310A24249-0-MTR</i>	<i>A02</i>







	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

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INVENTEC			
TITLE <i>Hello AMD discrete SLG3NB142V</i>			
SIZE A3	CODE CS	DOC. NUMBER <i>1310A24249-0-MTR</i>	REV A02
CHANGE by <i>David Cheng</i>		26-Apr-2011	
SHEET		57	OF 60

	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

www.aitech1.ru

INVENTEC			
TITLE <i>Hello AMD discrete</i>			
SIZE A3	CODE CS	DOC. NUMBER <i>1310A24249-0-MTR</i>	REV A02
CHANGE by <i>David Cheng</i>		26-Apr-2011	
SHEET		58	OF 60

	1	2	3	4	5	6	7	8	
A	<div>www.aitech1.ru</div>								A
B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

INVENTEC			
TITLE <i>Hello AMD discrete</i>			
SIZE A3	CODE CS	DOC. NUMBER <i>1310A24249-0-MTR</i>	REV A02
CHANGE by <i>David Cheng</i>		26-Apr-2011	
SHEET		59	OF 60

	1	2	3	4	5	6	7	8	
A	<div>www.aitech1.ru</div>								A
B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

INVENTEC

TITLE
Hello AMD discrete

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24249-0-MTR	A02

CHANGE by *David Cheng* 26-Apr-2011

SHEET 60 OF 60